Mitigation of short channel Effects Beyond Silicon: The comparative Meta-analysis of 14nm FinFETs and 2D Mos2 channel architectures

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Abstract
The long-running scaling of silicon CMOS technology to the 14nm node and beyond has exacerbated these important short-channel phenomena (Drain-Induced Barrier Lowering (DIBL) and gate leakage currents), which also exist with high-k interfacial layers. This paper presents a meta-analysis of recent experimental and theoretical results to evaluate the performance-limiting parameters of conventional 14 nm silicon FinFETs in comparison with the latest two-dimensional material-based Field-Effect Transistors (2D-FETs), using monolayer Molybdenum Disulfide (MoS2) as the channel material. By borrowing the low-dimensional thin, atomically smooth properties, and direct bandgap features of MoS2, in this theoretical case we observe the enhanced electrostatic gate control, which might effectively alleviate the basic issues of DIBL and tunneling leakage current to some extent for existing 3D silicon fin devices. The theoretical analysis covers these critical performance parameters: subthreshold swing, Ion/Ioff current ratio, and carrier mobility degradation under scaled supply voltage settings. The theoretical insights of this work furnish valuable insights about the enabling role of transition metal dichalcogenides (TMDCs) within the limits of silicon scaling fundamentals by providing a theoretically justifiable view for the future development of low-power and high-performance integrated circuit technologies and modeling paradigms.

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