GrapheneforUS

**MD MAHFUZUR RAHMAN**[1]
Amirjan Bin Nawabjan[2]
Department of Nano-Micro Engineering, Universiti Teknologi Malaysia, 81310 Skudai, Johor, MALAYSIA

mrmd4@graduate.utm.my

# Doped Graphene on Silicon FET for High Drain Current and Applications in RF And Logic Circuits

The Si-adsorbed and Si-substituted monolayer Si-doped graphene (Si:Gr) material has a range of structural and electronic features, according to recent researches. The Si:Gr demonstrates adatom-diversified geometric structure, silicon-carbon dominated energy bands, density of states projected from atom's orbit and charge concentration in space. The exploration of these critical physical characteristics generate distinct physical and electrical properties of the distinct material Silicon doped graphene (Si:Gr) permitting it to be used in semiconductor technology [1]. Due to the excellent carrier mobility and saturation velocity, graphene devices are very useful in RF applications. Recent studies suggest that utilizing bare silicon as a supporting substrate without an insulating layer under the graphene channel in conventional field effect transistor (FET), can result in high output resistance and voltage gain, which provides higher cut-off frequency comparing with conventional graphene-FET (GEFT) [2]. In this work, an N-channel GFET with printed channel length of 50nm has been designed with Si:Gr as channel material and the Si:Gr is deposited on lightly doped p-type silicon substrate eliminating the insulator layer. For optimum RF performance bottom gate with $SiO_2$ as gate dielectric has been utilized. The device has provided maximum cut-off frequency of 496GHz and Ion/Ioff ratio of $139.5x10^3$ (bottom gate, metallic contact) proposing a novel device for RF and logic circuit applications.

## References

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## Figures

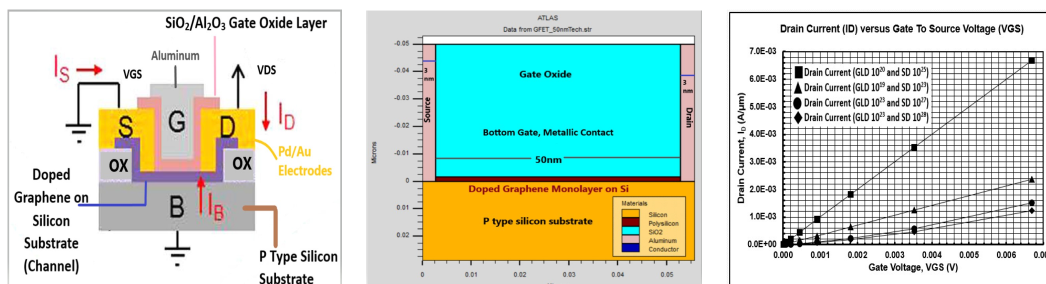


Figure01: (left) Theoretical structure of proposed device[2] (middle) simulated device (right) IV characteristics of the device at VDS = 0.2V

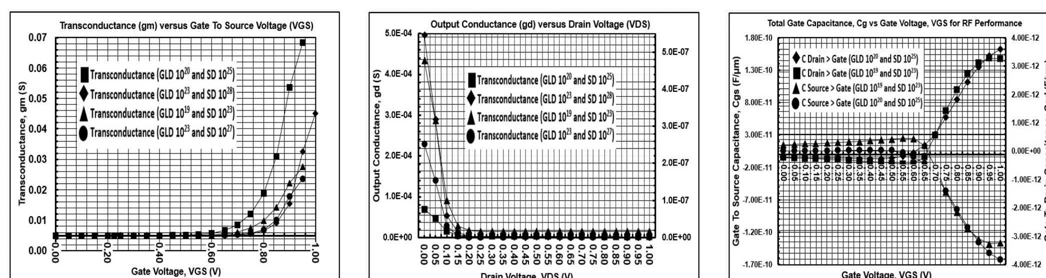


Figure 02: Transconductance vs gate voltage, Output conductance vs drain voltage and gate capacitance of the proposed device. Successful results verify the validity of the proposed device design.