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Density of Interface States in Layered-WSe_2 Semiconductor

Unlike conventional bulk materials, the physical characteristics of two-dimensional (2D) materials are tailored by thickness variation and the quality of interface formed with the immediate environments. [1,2] Here, we investigate the thickness dependent intrinsic and interfacial characteristics of WSe_2 with special focus on hBN/WSe_2 interface by performing capacitance-voltage (C-V) measurements. Our results show that the interface sate density (D_{it}) at the edge of WSe_2 band gap is drastically reduced from ~10^{13} to 10^{11} cm^{-2} eV^{-1} with the increase of WSe_2 thickness from few to multilayers. The high D_{it} in thin flake-based device demonstrate that the thin flake is more sensitive to the interface to induced strain from the substrate surface roughness, device processing defects, and intrinsic defect density at the WSe_2 surface. Therefore, our findings emphasize the need of low intrinsic defect density and interfacial defect density to fabricate the reliable and high-quality 2D devices. These results can be used to understand the intrinsic and interfacial properties of 2D materials and provide guidelines to design future reliable and doping-free 2D solid-state devices.

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References

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Figures

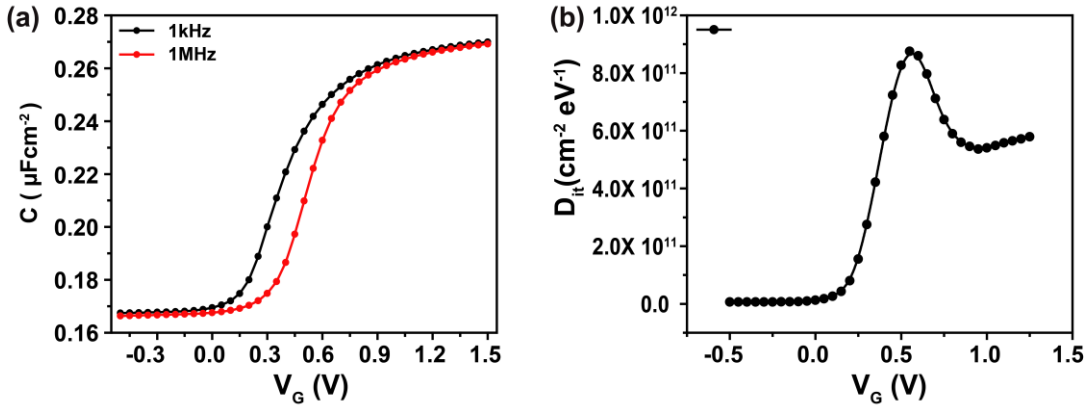

Figure 1: (a) C-V characteristics of the exfoliated n-type WSe_2 MIS capacitor at low 1 kHz and high 1 MHz frequencies.
(b) Extracted Dit as a function of applied VG of n-type WSe_2.