

Zheng Yang

Changsik Kim, Kwang Young Lee, Samudrala Appalakondaiah, Kenji Watanabe, Takashi Taniguchi, Euyheon Hwang, James Hone, and Won Jong Yoo
SKKU Advanced Institute of Nano Technology, 2066, Seobu-Ro, Jangan-Gu, Suwon-Si, Korea

yangzheng@skku.edu

Fermi Level Pinning-Free 1D Electrical Contact at a Metal-2D MoS₂ Junction

Currently 2D crystals are being studied intensively for use in future nano-electronics, as conventional semiconductor devices face challenges in high power consumption and short channel effects when scaled to the quantum limit. Toward this end, achieving barrier-free contact to 2D semiconductors has emerged as a major roadblock. In conventional contacts to bulk metals, the 2D semiconductor Fermi levels becomes pinned inside the bandgap, deviating from the ideal Schottky-Mott rule and resulting in significant suppression of carrier transport in the device. Here we achieve near-ideal alignment of the Fermi level with a pinning factor of 0.98, by employing a 1D edge contact scheme. Use of high work function palladium (Pd, 5.6 eV) achieved ambipolar contact to MoS₂, which typically shows unipolar n-type characteristics. Field-effect transistors (FET) with Pd edge contacts show high performance with hole mobility reaching $330 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ at 300 K with on/off ratios of 10^8 . The ideal Fermi level alignment allows creation of p- and n-type FETs on the same MoS₂ flake using Pd and molybdenum (Mo, work function 4.5 eV) contacts, respectively. This device acts as an efficient inverter – a basic building block for future 2D semiconductor integrated circuits -- with gain reaching 15 at $V_D=5 \text{ V}$.

Figures

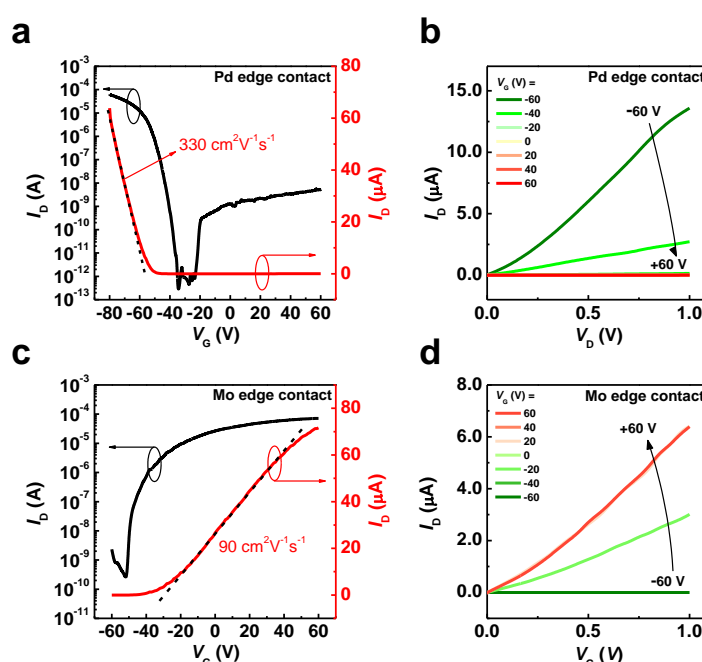


Figure 1: Electrical performance of Mo/ MoS₂ and Pd/ MoS₂ edge contact FETs. Transfer curves on the log (black) and linear (red) scales, for Pd (a) and Mo (c) at $V_D = 1 \text{ V}$ (Pd) and 2 V (Mo). Output curves with different gate voltages of Mo (b) and Pd (d). Mo edge contact FET ($L = 6 \mu\text{m}$, $W = 2 \mu\text{m}$). Pd edge contact FET ($L = 10 \mu\text{m}$, $W = 16 \mu\text{m}$).