

# High-Performance and Energy-Efficient Sub-5 nm 2D Double-Gate MOSFETs Based on Silicon Arsenide Monolayers

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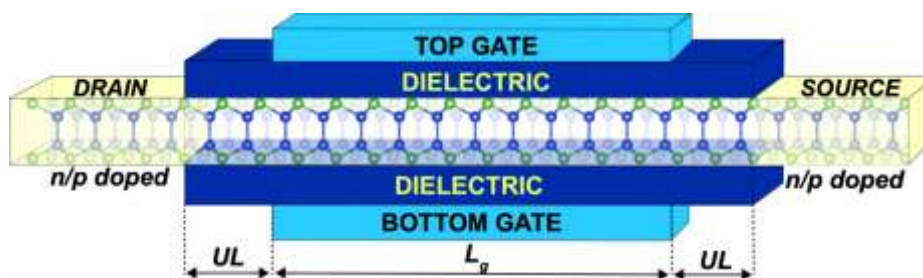
## Abstract

As the demand for high-performance, energy-efficient transistors grows, traditional silicon-based MOSFETs face significant scaling limitations[1]. To overcome these challenges and sustain advancements in semiconductor technology, new materials and device architectures are being explored[2]. In this study, sub-5nm double-gate metal-oxide-semiconductor field-effect transistors (MOSFETs) based on two-dimensional (2D) SiAs are investigated using first-principles calculations and the Non-equilibrium Green's function (NEGF) formalism to assess their potential as a high-performance alternative. SiAs monolayers exhibit an indirect bandgap of 1.58 eV and demonstrate promising electronic properties. Key performance metrics such as the on/off current ratio, subthreshold swing (SS), gate capacitance ( $C_g$ ), intrinsic delay time ( $\tau$ ), and power-delay product (PDP) are evaluated. Devices with 1 nm and 2 nm underlap (UL) structures show enhanced performance, achieving on-state current ( $I_{on}$ ) values up to  $1206 \mu\text{A}/\mu\text{m}^{-1}$  meeting ITRS-2028 high-performance (HP) standards. The SS ranges from 112 to 142 mV/dec, and minimized delay and power-delay products indicate the suitability of SiAs transistors for ultra-scaled, energy-efficient applications. These results suggest that 2D SiAs transistors offer a promising solution to the scaling challenges of traditional MOSFET technologies, with potential for future semiconductor innovations.

## References

- [1] Theis, T.N. and Solomon, P.M., Science, 327.5973 (2010), 1600-1601.
- [2] Franklin, A.D., Science, 349.6249, 2015, p.aab2750.

## Figures



**Figure 1:** Device model of double-gate monolayer SiAs MOSFET.