

Mobility Optimization by Thermal Annealing in CMOS-Integrated Graphene FETs

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State-of-the-art silicon-based modulators cannot simultaneously meet the bandwidth and power-efficiency requirements of future data transmission systems, motivating the integration of high-mobility materials such as graphene into CMOS environment [1]. However, mobility in CMOS-integrated graphene devices is significantly degraded from its theoretical value. To address this, back-gated graphene field-effect transistors (GFETs) were fabricated on 200 mm SiO₂/Si wafers with Pd/Au and Ni edge contacts and Si₃N₄ passivation. We systematically investigated the impact of consecutive annealing steps in N₂ atmosphere up to 300 °C on carrier mobility. The maximum TLM mobility for holes (electrons) is achieved after annealing at 200 °C for Pd/Au contacts, reaching 1240 (1780) cm²/Vs, and after annealing at 150 °C for Ni contacts, reaching 590 (850) cm²/Vs. Raman studies of graphene show a decreasing defect ratio I_D/I_G with increasing annealing temperature, indicating an improved quality. Furthermore, Raman mapping of graphene with Pd/Au contacts reveals narrow distributions of the 2D and G peak positions, whereas Ni contacts result in broader peak distributions accompanied by increased p-doping compared to Pd/Au. This project has received funding from the European Union's Horizon Europe research and innovation program under grant agreements No 101120938 (GATEPOST) and 101189797 (2D-PL).

References

- [1] M. Romagnoli, V. Sorianello, M. Midrio, F. H. L. Koppens, C. Huyghebaert, D. Neumaier, P. Galli, W. Templ, A. D'Errico, and A. C. Ferrari, *Nature Review Materials*, 3 (2018) 392 - 414

Figures

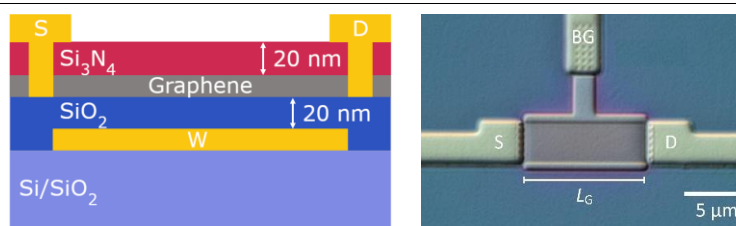


Figure 1: Cross-section of the investigated graphene field-effect transistors (left). Optical image of the graphene channel area with source (S), drain (D) and back-gate (BG) contact pads (right).

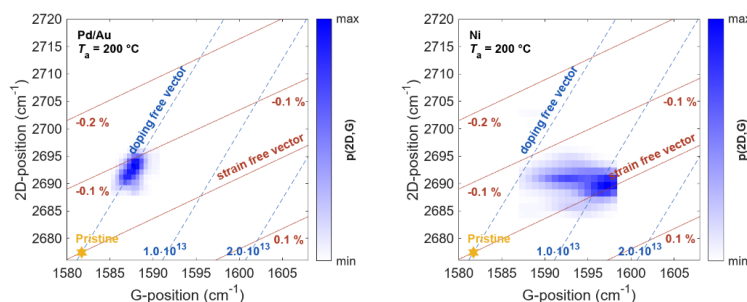


Figure 2: Probability density $p(2D,G)$ of the 2D and G peak positions showing the correlation of doping and strain at $T_a = 200$ °C for Pd/Au (left) and Ni (right).