Synthesis and Device Integration of 1D-Te/2D-MoS_2 van der Waals Heterostructures

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The p-n junction is a fundamental building block of many important electronic devices, including LEDs, solar cells, photodiodes, and BJTs. vdW materials offer a promising platform [1] for studying nanoscale p-n junctions, as the weak interlayer bonding between adjacent layers creates defect-free interfaces, circumventing the lattice-matching constraints typically encountered in epitaxial heterojunctions [2]. We report a sequential two-step vapor deposition technique for growing in situ mixed-dimensional heterostructures, specifically 1D p-type Te nanowires (via PVD) on 2D n-type MoS_2 flakes (via CVD) [3]. This growth technique produces large scale, high-quality, atomically sharp 1D/2D interfaces on SiO_2/Si substrates that overcome the hazardous effects of transfer residues. The assembled samples serve a twofold purpose. First, the electrical transport measurements reveal a well-defined narrow depletion region (<10 nm) with built-in potential 0.19 V across the junction. These heterostructures function as back-gate-tunable p-n junction diodes with rectification ratio ~200. Furthermore, charge transfer at the heterointerface is validated via Raman spectroscopy and Kelvin probe force microscopy. Second, the nonhybrid regions on the substrate, isolated Te and MoS_2 microstructures from the same growth run, were utilized to fabricate p- and n-type FETs, respectively. By employing ionic-liquid gating, we demonstrate low-power CMOS inverters and basic logic-gate operations. This work showcases a unified platform for integrating analog and digital circuits.

References

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Figures

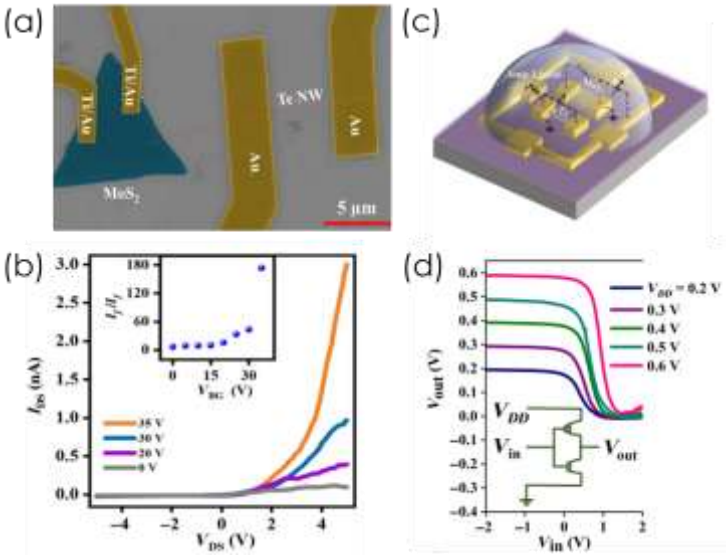

Figure (a): False-colored SEM image of a tasted device fabricated by electron beam lithography. **Figure (b):** Plots of I-V curves at different back-gate voltages measured across the p-n heterojunction device. **Figure (c):** Schematic of an IL-top-gated Te NW and MoS_2 FET. **Figure (d):** Voltage transfer (V_{in}-V_{out}) CMOS inverter at different V_{DD} values. The inset shows a schematic of the electrical configuration for the CMOS inverter.