Scaling and integration of Ag-based threshold-type switching devices in hexagonal boron nitride at CMOS back-end-of-line

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Threshold-type resistive switching (RS) is essential for selector devices and electronic neurons [1], but Ag-based diffusive memristors are typically demonstrated on large-area devices (>1 μm^2) fabricated on unfunctional substrates (SiO_2/Si), limiting their relevance for integrated systems [2]. In particular, switching behaviour, endurance, and operating conditions do not scale predictably with device size or integration environment [3-4]. Here, we demonstrate Ag-based threshold switching devices using multilayer hexagonal boron nitride (h-BN) integrated at the back-end-of-line (BEOL) of CMOS microchips, with device areas down to ~0.05 μm^2. While large-area Ag/h-BN/Ag devices fabricated on SiO_2/Si exhibit forming-free volatile switching at low V_{SET} (~0.47 V) and high endurance up to ~9×10^6 cycles (**Fig. 1**), direct on-chip integration leads to the loss of threshold switching due to increased energy required for filament formation in reduced device dimensions (**Fig. 2-3**). Removing the Ag layer, results in the absence of RS completely, and only erratic resistance fluctuation is present (**Fig. 4**). We show that this limitation can be overcome by engineering the top electrode composition. By introducing a limited-volume Ag layer (~1 nm) within the top electrode, we control the formation of conductive nanofilaments and recover stable volatile switching in fully integrated 1T1R cells. The optimized devices exhibit forming-free operation, switching voltages below 1.5 V, and endurance up to ~4 × 10^6 cycles (**Fig. 5**). These results demonstrate that switching behaviour in diffusive memristors is strongly dependent on device scaling and integration conditions, and cannot be extrapolated from large-area devices. Finally, we validate the use of these devices as leaky integrate-and-fire neurons in spiking neural networks, achieving correct classification in 94% of cases. This work establishes a pathway for integrating 2D-material-based threshold switching devices into CMOS platforms for neuromorphic computing.

References

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[4] Chen, A. et al. 71st Device Research Conference, Notre Dame, IN, USA, 2013, 181-182.

Figures

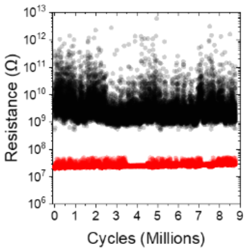

Fig 1: Endurance of a device on SiO_2/Si.

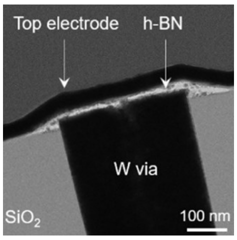

Fig 2: Cross-sectional TEM of on-chip device.

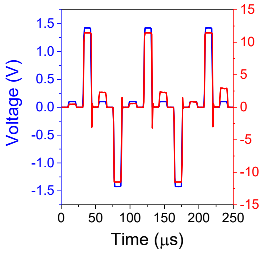

Fig 3: Loss of threshold switching on-chip.

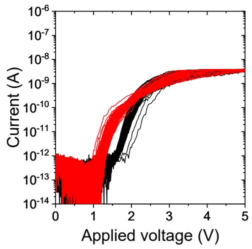

Fig 4: Ag removal resulting in the absence of RS of devices on-chip.

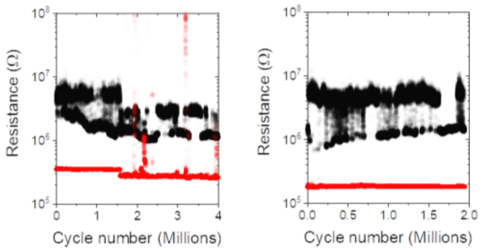

Fig 5: Endurance plots of engineered devices on CMOS microchip.