Van der Waals Integration of Two-Dimensional Semiconductors with Free-standing Ferroelectric Oxides for Future Electronics

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Abstract: Ferroelectric materials play a vital role in a wide range of applications in semiconductor technologies. Devices based on ferroelectrics integrated with twodimensional (2D) materials extend the possibilities for tuning various electronic properties of semiconductors through the virtue of ferroelectric polarization switching. The interfaces between 2D materials and ferroelectric oxides suffer from traps and defects and are restricted by lattice matching constraints. Recently, van der Waals (vdW) integration of 2D materials and free-standing complex oxides has been shown to be a promising solution [1,2]. In this work, we explored the potential of vdW integration of 2D semiconductors with freestanding functional oxides for 2D field-effect transistors (FETs). Thin films of various oxides, including SrTiO₃ (STO) and BiFeO₃ (BFO), were successfully grown using pulsed laser deposition, producing high-quality free-standing films. These free-standing films were integrated into FET device heterostructures where MoS₂ was used as the channel. The MoS₂ FETs with free-standing STO gate dielectric showed notable performance and a low subthreshold swing of 74 mV/dec compared to those prepared on conventional SiO₂, due to the high dielectric environment provided by STO. Preliminary work on STO provided insights into incorporating free-standing ferroelectric oxides into the gate stack to realize Ferroelectric FET (FeFET) and Negative Capacitance FET (NCFET). Ferroelectricity in freestanding films was demonstrated using piezo force microscopy. Subsequently, all vdW integrated MoS₂ FETs were fabricated with free-standing ferroelectric oxide gate dielectric. The fabricated devices showed remarkable dielectric stability (4 MV/cm) and ferroelectric switching. Further, they exhibited sub-60 mV/dec operation with low operation voltage and on-off current ratio greater than 10⁵. This approach of vdW engineering of 2D materials with free-standing oxides demonstrates the feasibility of achieving good interface quality and various property tunability for future electronic applications.

References

- [1] Huang, JK., Wan, Y., Shi, J. et al. Nature 605 (2022), 262–267.
- [2] Puebla, S., Pucher, T., Rouco, V. et al. Nano Letters, 22,18 (2022) 7457–7466.