Numerical Analysis of Charge Transport Behavior in WSe_2 multilayers for High-Performance Transistor Optimization

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Two-dimensional (2D) van der Waals (vdW) materials have gained attention as promising alternatives to silicon due to their atomically thin nature, lack of dangling bonds, and chemically inert surfaces, which minimize surface scattering and interface defects[1]. Their unique properties, including tunable band gaps, strong exciton binding energies, and excellent electrostatic control, make them well-suited for high-performance nanoelectronic and optoelectronic devices[2]. However, the electronic transport properties of 2D vdW materials are strongly influenced by factors such as film thickness, surface cleanliness, unintended doping, electrostatic gate bias, contact resistance, and dielectric properties[3]**¡Error! No se encuentra el origen de la referencia.**. To gain a deeper insight into the charge transport mechanisms, we performed numerical simulations based on the Thomas-Fermi charge screening theory and a ladder resistive equivalent model to systematically investigate how variations in contact resistance and interlayer resistance affect the current distribution. In addition, we simulated charge behavior as a function of WSe_2 thickness and electrode structure, demonstrating the feasibility of simulating various 2D vdW materials by adjusting key parameters. By addressing critical challenges such as contact resistance, interlayer resistance, and electrostatic gate control, our results provide essential insights into charge transport in 2D vdW materials. These findings contribute to the optimization of WSe_2 layer thickness for field-effect transistors and advance the design of vdW-based nanoelectronic devices.

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Figures

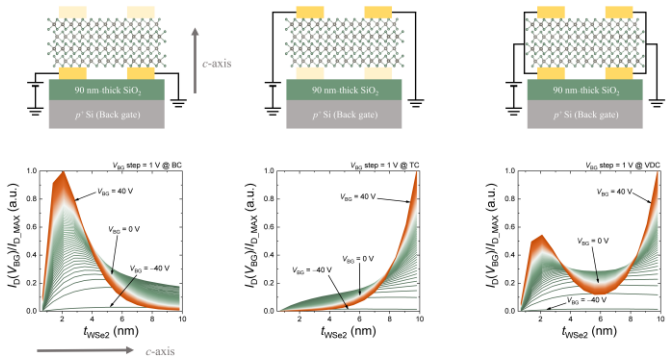

Figure 1: Schematic illustrations for (a) top contact (TC), (b) bottom contact (BC), and (c) vertical double side contact (VDC), respectively. Numerically simulated the thickness-dependent $I_D(V_{BG})/I_{D\_MAX}$ of 10 nm-thick WSe_2 with respect to (d) TC, (e) BC, and (f) VDC using a V_{BG} range of -40 to 40 V in 1 V steps.