High-Quality, Ultra-Thin Dielectric Integration on Graphene Enabled by Plasma ALD

Authors: Sarah Riazimehr[a]
Ardeshir Esteki[b], Gordon Rinke[c], Martin Otto[c], Bianca Robertz[c], Zhenxing Wang[c], Max C. Lemme[b, c], Harm Knoops[a]
a) Oxford Instruments Plasma Technology, Govier Way, Bristol BS35 4GG, United Kingdom
b) Chair of Electronic Devices, RWTH University, Otto-Blumenthal-Str. 2, Aachen, Germany
c) AMO GmbH, Otto-Blumenthal-Str. 25, Aachen, Germany
sarah.riazimehr@oxinst.com

The performance potential of nanoelectronic devices based on two-dimensional (2D) materials remains largely unexplored due to the lack of scalable, high-quality insulators[1]. In this presentation, we propose a scalable approach for the deposition of high-quality dielectric on graphene. In previous year, we introduced an in-situ damage-free dielectric deposition process utilising a nonstoichiometric AlOX seed layer grown under mild plasma conditions[2] (see Figure 1a and b). In this presentation, we demonstrate the effectiveness of this approach on top-gated graphene field-effect transistors (GFETs). Dual-gate measurement devices fabricated using our method achieve an equivalent oxide thickness (EOT) below 5 nm (Figure 1c and d) and an electric field strength exceeding 11 MV/cm (Figure 1e) on a wafer scale. Additionally, we will discuss the impact of in-situ cleaning and post-deposition annealing on device performance, highlighting the potential of this method for other 2D materials and alternative dielectric systems.

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References

[1] Y. Illarionov et al., Nat Commun, 11 (2020) 3385
[2] H. Knoops et al., J. Vac. Sci. Technol. A, 39 (2021) 062403

Figures

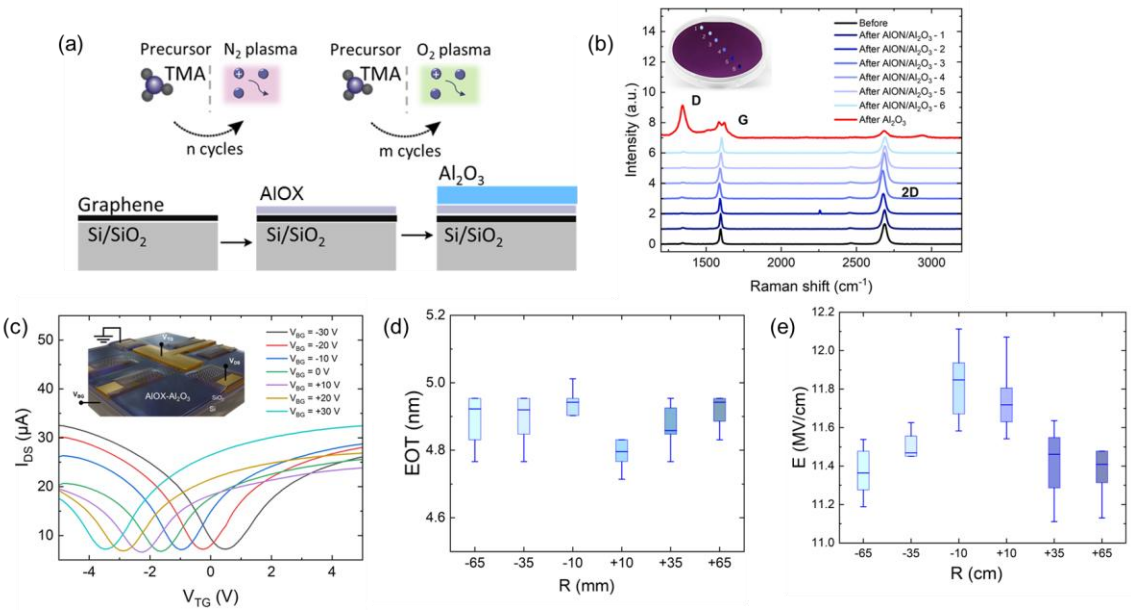

Figure 1: (a) Process scheme of AlOX seed-layer deposition and Al_2O_3 plasma ALD. (b) Raman spectra across the wafer radius (R) for Gr/SiO2/Si wafers before (black) and after Al_2O_3 deposition without (red) and with (blue) AlOX seed-layer. (c) Dual-gated current–voltage plots for a GFET. Inset: Schematic of a dual-gated GFET in a two-point measurement. Statistical extraction of (d) EOT and (e) the electric field strength over R.