Doping Using Ion-Charged Dielectric for CVD Graphene <120 Ω/□

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Transparent conducting electrodes (TCEs) are a major contributor toward losses in optoelectronic devices such as solar cells and LEDs [1], mainly due to the challenge of achieving broadband transmittance with low sheet resistance (R_{sheet}) in conventional metal-oxide TCEs. The best-performing TCEs also contain indium, limiting scalability [1]. Graphene offers unique advantages: >95% transmittance, 10-100× higher mobility than metal-oxides, and sustainable production, but its R_{sheet} remains too high [2]. While doping can lower its R_{sheet} to values comparable to that of metal-oxides, existing methods are typically unstable and reduce transmittance and mobility. Here, we propose a stable graphene doping technique using ion-charged dielectrics (ICDs), for low R_{sheet} and high transmittance. To introduce charge into a dielectric, a KCl precursor was deposited on SiO_2/Si. Following ref. [3], K^+ ions were migrated to the SiO_2/Si interface using a corona anneal. CVD-graphene was then wet-transferred to the K^+:SiO_2. Figure 1.a depicts the graphene R_{sheet} variations over time under bias-annealing. The device was first annealed in vacuum at zero bias to remove atmospheric contaminants. A reverse bias was applied at high temperatures, migrating K^+ toward graphene. With increased bias, more ions were migrated, reducing R_{sheet}. Capacitance-voltage measurements confirmed ion movement, and FET devices (Figure 1.b) revealed n-doping to $>6\times10^{12}$ q/cm^2, with no significant mobility reduction. Spectrophotometry revealed that graphene's >95% transmittance was preserved. After two months, the R_{sheet} remained within ~10-15% of the doped value. This doping reduced the R_{sheet} achieved to among the lowest large-area CVD-graphene R_{sheet} reported on SiO_2 [4], at ~117 Ω/□ in the champion case, highlighting its strong competitiveness with indium tin oxide and its potential as a novel doping technique for 2D materials for optoelectronics and applications in integrated circuits.

References

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Figures

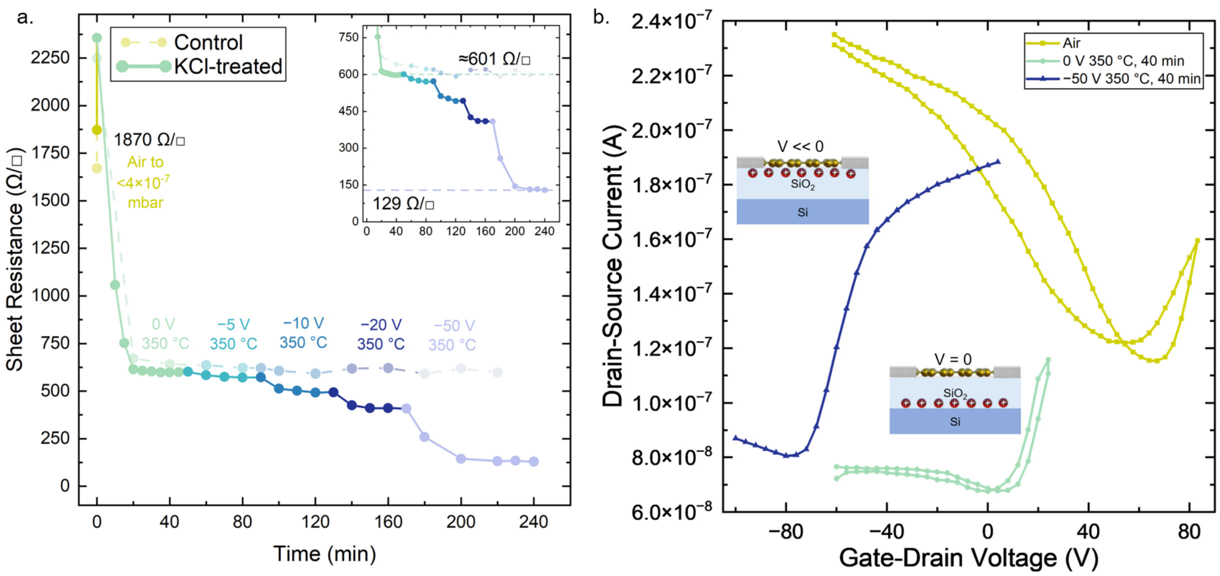

Figure 1: Graphene on KCl-treated or untreated substrate before and after bias-temperature stress, in vacuum. a. R_{sheet} measurements. b. FET device measurements.