Temperature and bias-dependent capture-emission time maps in electrolyte-gated graphene field-effect transistors

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Electrolyte-gated graphene field-effect transistors (EG-gFETs) have recently been proposed as platforms for sensing biomolecules due to their high chemical stability and biocompatibility, electron/hole mobility, and sensitivity to the external environment.
The most common biodetection method is tracking the device's transfer curve minimum conductance point (Dirac Point) shift, which occurs in the presence of the analyte of interest [1]. However, the translation of the transfer curves can be challenging to detect due to the intrinsic electrical instability of the devices. For example, it has been observed that repeated acquisitions of the transfer curve cause a Dirac Point drift, even in the absence of an analyte (Fig.1a). This instability is believed to be caused by the charge carriers traffic between the graphene channel extended states and localized states in the oxide layer underneath [2]. In this case, charges that remain progressively trapped in the oxide will locally gate the graphene, shifting its Fermi level and moving the Dirac Point.
In this work, we have experimentally studied the response of the EG-gFETs under various stressing and relaxation conditions at different voltage bias values and temperatures (fig.1b). We fit all the experimental data with a previously developed analytical model based on charge trapping at the silicon oxide substrate defects in contact with the graphene channel (Fig.1c). In the model, the electron transitions require the absorption of phonons to overcome the energetic barrier leading to the new state. Consequently, the process is temperature and gate-bias-dependent.
The fitted parameters to the experimental data are then used for the first time to construct the Capture-Emission Time Maps (CET maps) [3] of the EG-gFET devices (Fig.1d). CET maps represent the capture/emission time distribution of the oxide defects, or in other words, how many of these defects are active at each timescale.
Studying these maps as a function of the bias and temperature allows us to gain insight into the best experimental conditions to minimize electrical noise during measurements and to propose improved detection protocols when using EG-gFETs.

References

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[2] Y. Illarionov et al, Nat Commun, 11, 3385 (2020)
[3] T. Grasser, Microelectronics Reliability, 52, pp. 39-70 (2012)

Figures

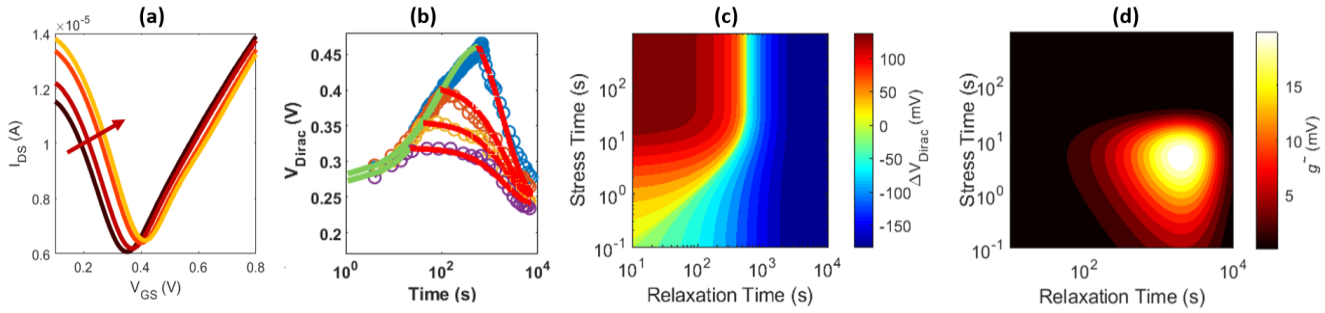

Figure 1: (a) EG-gFETs transfer curve drift with consecutive acquisitions; (b) Experimental data (symbols) and fitted model (lines) of the Dirac voltage (V_{DC}) drift of the EG-gFETs while acquiring consecutive transfer curves (stress period) and while letting the transistor relax; (c) Modelled drift of the Dirac voltage as function of the stress and relaxation time; (d) Capture-Emission Time (CET) map of the EG-gFET.