Next generation electronics enabled by growth-based monolithic integration of 2D materials

Jeehwan Kim
Massachusetts Institute of Technology
jeehwan@mit.edu

Two-dimensional (2D) semiconductors hold significant promise as a replacement for silicon in gate lengths below 10 nm, owing to their ability to sustain mobilities exceeding 100 $cm^2/V \cdot s$, compared to silicon, which degrades to below 10 $cm^2/V \cdot s$ in the same regime. Additionally, unlike silicon, 2D semiconductors eliminate the need for high-temperature doping activation, as metallization inherently forms the source and drain regions. This unique property enables seamless, wafer-free monolithic integration of logic and memory devices.

Despite their potential, the performance of state-of-the-art 2D transistors still lags behind modern silicon-based transistors. Key challenges include the inability to grow single crystals on silicon substrates, high contact resistance compared to 3D semiconductors, defective gate stack interfaces, and difficulties in achieving substantial doping activation [1]. Overcoming these hurdles is essential for realizing wafer-free monolithic 3D integration of logic and memory, a paradigm shift in electronic systems.

In this presentation, I will discuss innovative approaches of our team to addressing these challenges and share insights into the future outlook for 2D material-based electronics and their M3D based our signature low temperature confined growth technique [2,3].

References

[1] Nature Nanotechnology 19 (7), 895-906 (2024)
[2] Nature 614 (7946), 88-94 (2023)
[3] Nature 636 (8043), 615-621 (2024)