

Solution-Processable Two-Dimensional Materials for High-Performance Monolithic 3D Electronics

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Enabled by the rich electronic properties and unique defect dynamics, two-dimensional materials (2DMs) may offer excellent properties not seen in conventional bulk materials. A variety of insulators, conductors, and n/p semiconductors in atomically thin form offer a range of functionally engineered material that can be integrated with low-thermal budget. This makes them ideal material platforms for monolithic three-dimensional (M3D) integration of memory/logic devices compatible to process-temperature-limited on-chip metallized interconnects and low-k dielectrics. However, the current 2DM devices are often limited in large-scale circuit application, because of the high growth temperature and immature wafer-scale transfer technique. We have recently demonstrated wafer-scale implementation of 2D analog memory devices for monolithic 3D in-memory computation by solution processing technique (Nat. Comm., 2022 13, 1-9). We showed that the liquid-exfoliated 2D MoS₂ nanosheets with high crystal quality and clean van der Waals interfaces can be used as ideal building blocks for resistive-based memory. The abundant sulfur vacancies located at the edge sites offer a unique way for resistive switching modulation by engineering the ionic configuration associated with nanosheets size. Remarkably, the MoS₂ memristor exhibits forming-free switching with a high endurance of 1×10^7 cycles, low device-to-device variability, excellent retention and multibit analog resistive states. Our CNN implementation with the MoS₂ RRAM employs a unique conductance discretization based on variability and floating-point mapping techniques, effectively combating device variability and achieving a high accuracy of >98.02% in pattern recognition. Given the advantages with the colloidal 2DMs including CMOS compatibility, low-thermal budget, substrate agnosticism, low fabrication cost and wafer-scale scalability, we have demonstrated a monolithic 3D memory cube via layer-by-layer stacking of MoS₂ and metal connections in a transfer-free manner. In our recent research, we show the high-yield exfoliation of MoS₂, WS₂ and WSe₂ nanosheets from solution with high crystallinity and low defect density. Those nanosheets show promising results as channel materials for high-performance transistors. Given the capability of controlling the defect density through wet chemistry, we show that solution processed 2D materials with low thermal budget can be good candidate for both logic and memory devices in monolithic 3D electronics. In addition, our work offers feasibility for 3D circuits technique by seamless co-integration with Si-CMOS to enhance future on-chip computational functionality, where the memory-centric processing embraces the 3D circuit scaling.