Two-Dimensional Materials for Digital Electronics Beyond the 1 nm Technology Node

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The thickness of logic transistor channels needs to be drastically reduced as the lateral dimensions of Silicon transistors go below 1 nm technology node, to be able to pack more devices in smaller chips, increase their operating frequency and reduce their power consumption. Unfortunately, interface roughness severely reduces the carrier mobility when the transistor channel is thinned below 2 nm. In addition, the bandgap of silicon is too small to limit the leakage current.

This talk will summarize some of the work that our group at MIT has been doing to demonstrate the feasibility of using two-dimensional (2D) layered materials as the semiconducting channel in devices below 1 nm technology node. Molybdenum disulphide (MoS_2) for n-type channel transistors, and either tungsten diselenide (WSe_2) or tungsten disulphide (WS_2) for p-type channel transistors have ideal material properties to address some of the key challenges in future digital electronics [1]. Recent advances in material synthesis [2], key process modules [3] and device integration [4] will be discussed, as well as a calibrated design-technology co-optimization (DTCO) study.

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References

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Figures

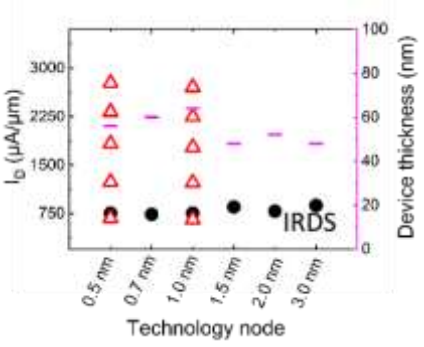

Figure 1: Simulations of the ON state current as a function of the number of MoS_2 channels for different technology nodes (red triangles). The minimum current levels per channel according to the International Roadmap for Devices and Systems (IRDS) are shown in black circles, together with the maximum height allowed per device (magenta lines).