Introducing 2D TMD in 300mm technologies. Updates on the TMD growth and deposition of the gate dielectric atop

Pierre Morin, Benjamin Groven, Henri Medina Silva, Pawan Kumar, Iryna Kandybka, Daire Cott, Alexandru Pavel, Zaoyang Lin, Dries Vranckx, Sebastiaan Nijs, Brecht de Vos, Kevin Deckers, Felix de Groef, Raf Rennen, Tinneke van Opstal, Alain Moussa, Tom Schram, Quentin Smets, Inge Asselberghs, Cesar Javier Lockhart de la Rosa, Gouri Sankar Kar.
imec, 75 kapeldreef, Leuven 3001, Belgium
pierre.morin@ imec.be

2D transition metal dichalcogenides (TMD) offer theoretically a better transport/electrostatic compromise than silicon at sub 10 nm logic gate length dimension, making them good candidate to intercept the logic roadmap for ultra scaled devices. Moreover, as 2D materials can be engineered to form devices at controlled thermal budget independently of the crystalline silicon substrate, TMD could be used in a shorter timescale to form new devices in the interconnect levels, to enrich technologies.
In parallel to the effort to demonstrate performant device in lab, we develop at imec a 300mm line and an integration platform to exercise these 2D materials in HVM compatible clean room and address several specific challenges related to this demanding environment. We will first report on recent progresses made related to TMD growth on our 200 and 300mm tools. We will share on process and precursor chemistry to enlarge the TMD grain size grown on sapphire or SiO2 substrate [1-4].
Integrating 2D materials on 300mm wafers with industrial requirements exacerbates the questions related to the interaction and the compatibility between 2D and 3D materials, during the fabrication of the technology. We will specifically share on the processes, tool challenges and maturity related to the deposition of 3D films such as high permittivity dielectrics on 2D TMD [5].
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References

[1] Iryna Kandybka & al. *ACS Nano 2024*, 18,4,3173-3186
[2] Alain Moussa & al. , Japanese J. Appl. Phys (2024)
[3] Benjamin Groven & al. TMDC workshop (2023)
[4] Henry Medina & al. SSDM (2023)
[5] Daire Cott & al, ALD conference (2023)

Figures

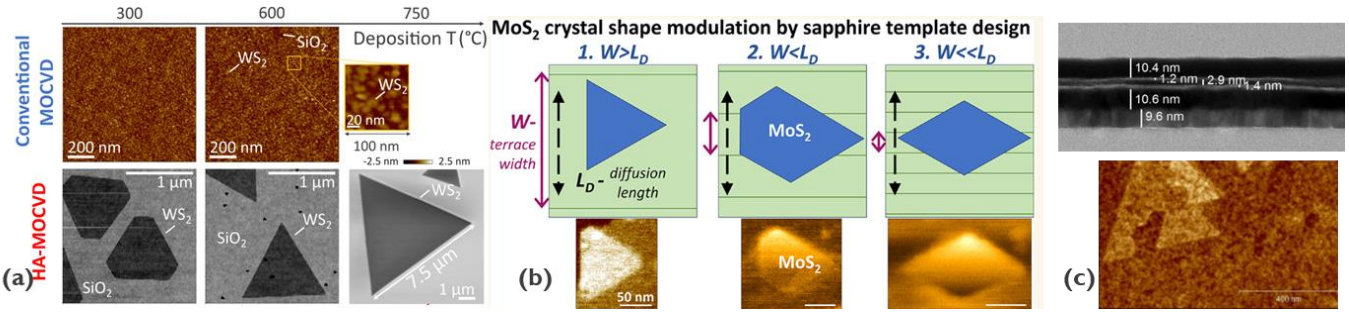

Figure 1: (a) Progress in halogen assisted CVD, (b) Anisotropic 2DCrystal Growth on stepped Sapphire Surface, (c) deposition of the gate dielectric on TMD over 300mm wafer.