Towards CMOS-compatible ALD-grown MoS_2 Devices for BEOL

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Among the most promising 2D materials for next electronic nodes are the transition metal dichalcogenides (TMDs), which present [1]: i) suitable bandgaps, ii) large effective masses reducing source-to-drain tunneling, iii) controllable thicknesses allowing excellent electrostatic control. However, difficulties in their fabrication, such as the scarcity of scalable fabrication methods [2], still suppose a bottleneck for their industrial implantation.

Here, we present MoS_2 back-gated devices synthesized via ALD through $[(NtBu)_2(NMe_2)_2Mo]$ and H_2S precursors [3] accomplishing the CMOS compatible criteria (direct synthesis below 450ºC). The process was carried out directly on Si/90nm-SiO_2 wafers (100 mm) controlling the final MoS_2 thickness as a function of the number of cycles at a fixed temperature of 370ºC. Different wafer colours presented in Figure 1.a can be considered as a signal of variety deposited layer thicknesses or absorbance properties. The corroboration of the synthesized MoS_2 layer was performed through Raman characterization in Figure 1.b. The spectrum shows the three characteristic peaks: one appearing around 509 cm-1, associated with the presence of Si/SiO_2 beneath the MoS_2; and the two peaks corresponding to the in-plane (E_{2g}) and the out-of-plane (A_{1g}) vibrational modes produced by 2H-MoS_2 crystals. Regardless the number of cycles employed in the synthesis, samples exhibit a separation of 24 cm^{-1}, resembling multi-layer material. In Figure 1.c, the atomic force microscopy topography of an etched device corroborates the presence of around 10 nm-thick MoS_2 layer in a 90 cycles sample. Evaluation of the MoS_2 sheet resistivity was directly carried out through 4-probe characterization without any processing. Sheet resistance divided by the form factor ($F \sim \pi/\ln(2)$) as a function of the synthesis parameters is presented in Figure 1.d suggesting resistivities above the MΩ orders. Note that the sample is characterized at zero gate bias. Increasing the number of cycles and reducing the synthesis temperatures seems to conduct a material conductivity improvement. Optimizing the fabrication process to reduce the contact and sheet resistance together with the increase of the carrier density is mandatory for a potential technology implantation.

References

[1] C. Huyghebaert et al., 2018 IEEE IEDM, p. 22.1.1-22.1.4.
[2] Z. Ahmed et al., 2020 IEEE IEDM, p. 22.5.1-22.5.4.
[3] A. Sharma et al., Nanoscale, vol. 10, no. 18, pp. 8615–8627, 2018.

Figures

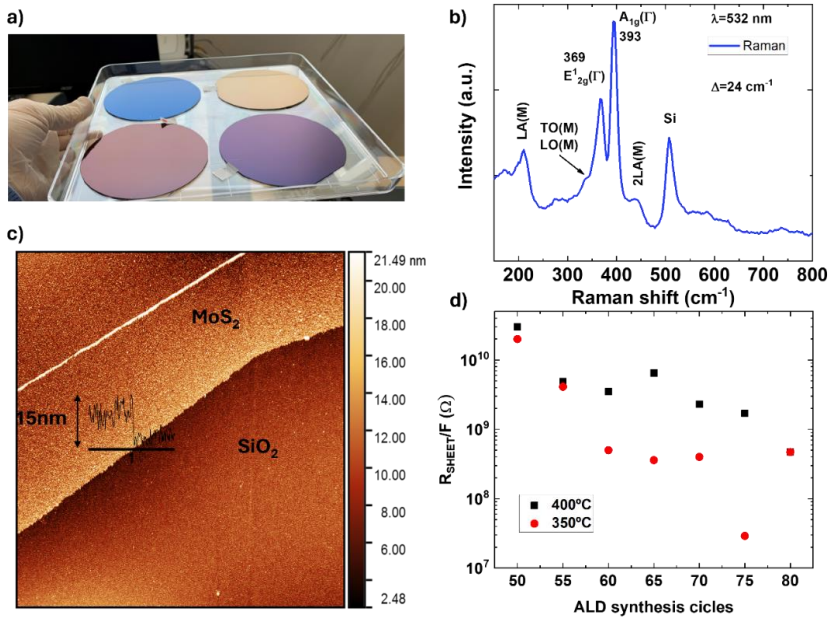

Figure 1: a) ALD-grown MoS_2 layers with increasing number of cycles on 100mm SiO_2/Si wafers. b) Raman spectrum for a 90 cycles MoS_2 layer (~15nm-MoS_2). c) AFM topography of an etched area. d) Four-probe sheet resistance for different number of cycles and temperature.