

# Resistive switching in graphene: A theoretical case study on the alumina-graphene interface

Renan P. Maciel<sup>1</sup>

Olle Eriksson<sup>1</sup>, Yaroslav O. Kvashnin<sup>1</sup>, Danny Thonig<sup>1,2</sup>, Daria Belotcerkovtceva<sup>1</sup>, M. Venkata Kamalakar<sup>1</sup>, and Chin Shen Ong<sup>1</sup>

<sup>1</sup> Department of Physics and Astronomy, Uppsala University, Box 516, SE-75120 Uppsala, Sweden

<sup>2</sup> School of Science and Technology, Örebro University, Fakultetsgatan 1, SE-70182 Örebro, Sweden

Organization, Address, City, Country (Century Gothic 10)

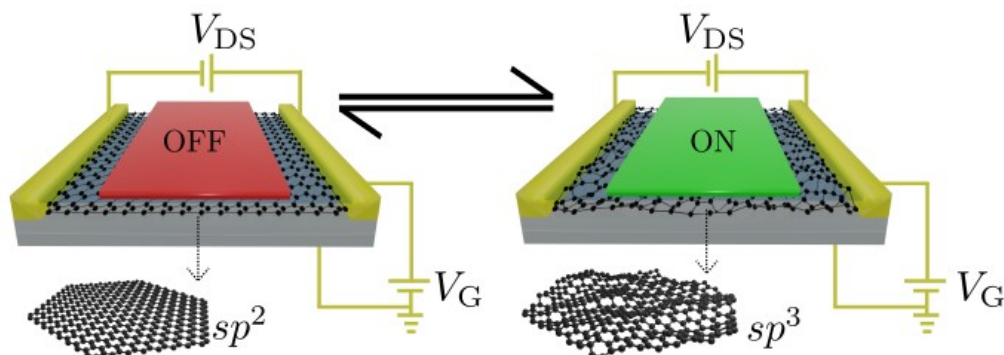
[renan.maciel@physics.uu.se](mailto:renan.maciel@physics.uu.se)

Neuromorphic computing draws inspiration from the structure of the human brain to develop devices that are energy efficient. The adaptability of synapses is fundamental in neuromorphic computing[1-2], achievable via memristive (memory resistance) switching mechanisms [3]. Specifically, memristors based on graphene exhibit the capability for nonvolatile multibit resistive switching, coupled with high endurance. Our research employs first-principles calculations to explore the structural and electronic characteristics of graphene interfaced with a thin alumina layer. We present how charge doping can be utilized to manipulate the interfacial covalency between these layers, allowing for reversible transitions between conductive and resistive states in graphene. Additionally, we propose that stabilizing this mechanism is feasible through the p-type doping, which could be achieved by the presence of natural defects, the neutralization of dangling bonds, or through targeted defect engineering.

## References

- [1] Wang et al. Nature Electronics 5, 870–880 (2022)
- [2] Marković et al., Nature Reviews Physics 2, 499–510 (2020)
- [3] Rao et al. Nature Machine Intelligence 4, 467–479 (2022).
- [4] Maciel, Renan P., et al. Physical Review Research 5.4 (2023): p.043147.

## Figures



**Figure 1:** Design of the graphene-based memristor. Red and green represent electrodes for triggering graphene's resistive and conductive states with voltage pulses. The semitransparent alumina layer is shown for clarity, positioned between graphene and the gold contacts.  $V_{DS}$  indicates the drain-to-source voltage, and  $V_G$  refers to the gate voltage.