# Contact resistance engineering in WS2-based FET with MoS2 under-contact interlayer – statistical approach

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The primary challenge in the fabrication of 2D material-based devices lies in achieving low-resistance contacts. Widely used methods of metal deposition (e.g., e-beam evaporation) damage the structure of TMD materials and lead to the Fermi level pinning (FLP) effect at the metal/semiconductor junction. This effect makes Schottky barrier height independent from a metal work function, hindering the design of efficient FETs. Recently, several approaches have been investigated to address this issue and the FLP effect has even been used to create new strategies for contact engineering in TMD-based devices [1][2]. Unfortunately, those new strategies are often evaluated based on the performances of only a few devices, which may hide issues related to performance reproducibility and potential inhomogeneity of 2D materials.
In this work, we first demonstrate an Au/$MoS_2$/$WS_2$ (Fig. 1a) junction to effectively reduce contact resistance in monolayer WS2-based field-effect transistors. The $MoS_2$ monolayer, acting as an under-contact interlayer, enables using FLP to our advantage for achieving favorable band alignment at the junction. In addition, a gold tape-based transfer method was created to fabricate $MoS_2$/$WS_2$ van der Waals heterostructures. To access reproducibility and thoroughly investigate the influence of the interlayer on the device's performance, we examined key FET performance indicators of 80 devices fabricated on monolayer WS2 with $MoS_2$ under-contact interlayer and 80 devices fabricated on only $WS_2$ monolayer. The architecture of our FET (Fig. 1b) allows for a reliable determination of the contact resistance, which decreased by over 60 % (Fig. 1c) due to the influence of the $MoS_2$ interlayer.

## References

[1] K. Murali, et al., Advanced Functional Materials, 31 (2021), 2010513.
[2] K. Andrews, et al., ACS Nano, 14 (2020), 6232

## Figures

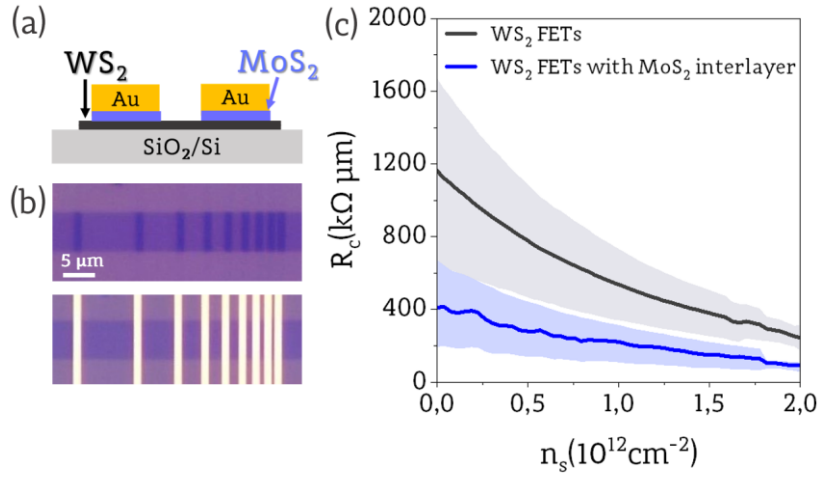


**Figure 1:** a) Schematic of the $WS_2$ FET with $MoS_2$ under-contact interlayer, b) (Top) Optical image of the van der Waals heterostructure with various spacing between $MoS_2$ stripes placed on the $WS_2$ layer. (Bottom) Optical image of the device with gold contacts evaporated on heterostructure areas, c) Mean contact resistance and standard deviation dependence on various carrier concentrations.