Gate-injection synaptic transistors based on 2D van der Waals heterojunction with band offset

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Abstract (Century Gothic 11)
Since the introduction of the memristors with combined characteristics of a resistor and memory in 1971, significant attention has been directed towards its application in alleviating the von Neumann Bottleneck within contemporary electronics. This unique attribute of the memristor has led to its utilization as a synaptic device, with the purpose of emulating the efficient calculation algorithms employed by the human brain. The successful implementation of such a neuromorphic system hinge on achieving a gradual change in conductance while maintaining symmetry between potentiation and depression phases. Here, we report gate-injection synaptic transistors with a linear conductance update driven by thermionic emission rather than Fowler-Nordheim tunneling by replacing the blocking layer with a 2D semiconductor material. To enhance the linearity and symmetry of pulse updates in synaptic transistors, we employed three-terminal synaptic transistors consisting of channel, dielectric, charge storage layer, and blocking layer of 2D materials, specifically transition metal dichalcogenides (TMDCs). We use MoS2 as a channel and charge storage layer, and MoSe2 as a blocking layer to make type II van Der Waals (vdW) heterojunction. We also fabricated device with WSe2 as blocking layer and examine correlation between band offset and conductance linearity. Our work demonstrates the potential of two-dimensional materials in memristor research in that the band offset of two-dimensional heterojunctions can be used to tune the linearity, symmetry of pulse updates, and responsiveness of memristor devices to pulses.

References

Figures

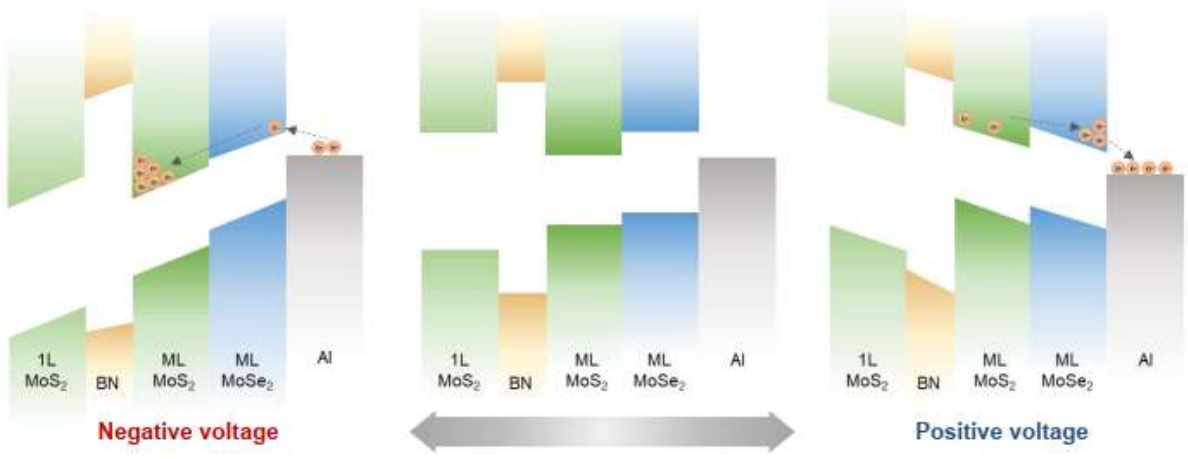

Figure 1 : Mechanism of Gate- injection synaptic transistors based on 2D van der Waals heterojunction