Dual-gating 2D p-FETs achieved via van der Waals integration and contact spacer doping

Min Sup Choi[1]
Tien Dat Ngo[2], Tuyen Huynh[2], Yoona Hwang[1], Won Jong Yoo[2]
[1]*Chungnam National University, Daejeon, Republic of Korea*
[2]*SKKU Advanced Institute of Nano Technology, Suwon, Republic of Korea*
goodcms@cnu.ac.kr

Abstract

The absence of high-performance p-type field effect transistors (p-FETs) is hindering the advancement of 2D materials in emerging CMOS technology. One potential remedy for this issue involves employing a top-gate (TG) configuration with a p-doped spacer region[1]. However, devising and processing such a device to establish gate stacks pose significant challenges in achieving optimal p-FETs and PMOS inverters. In this study, we propose an innovative approach to attain dual-gating lateral p^+– p – p^+ junction WSe_2 FETs with precise control over TG length. Our method integrates self-aligned TG stacks via van der Waals (vdW) integration, coupled with oxygen plasma doping in the contact spacer areas. Unlike conventional methods, we demonstrate effective electrostatic modulation of 2D p-FETs through the implementation of TG stacks. Utilizing self-aligned TG as a doping mask yields a high on-off current ratio exceeding 10^7, a minimal dual-gating subthreshold swing (SS) of 79 mV dec^{-1}, and a near zero threshold voltage (V_{th}) in WSe_2 p-FETs. Reducing the TG length to 300 nm yields a substantial on-state current of around 100 μA $μm^{-1}$, while preserving an on/off ratio of 10^4. Furthermore, we validate the effectiveness of our approach by demonstrating a PMOS inverter with remarkably low power consumption, approximately 4.5 nW.

References

[1] T. D. Ngo et al., Advanced Science, 9 (2022) 2202465 (Century Gothic 11) Indicate references with sequential numbers within [square brackets].