Contact Resistance and Oxide Trap Effects on Charge Fluctuation of WSe_2 Multilayers

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Thus far, various experimental and theoretical studies have demonstrated the modulation of conducting channel distribution along the thickness of 2D multilayers primarily by attributing to the electrically tunable high interlayer barrier and the thickness-dependent carrier mobility. However, high contact resistance exhibited at the metal-to-2D semiconducting multilayers with the inherent vertical interlayer tunneling barrier between neighboring layers hinders a clear feature of vertical charge carrier transport. In this poster, we demonstrate the effects of channel access contact resistance on the vertical carrier density profile along the thickness and surface defect density in WSe_2 multilayers. The constructed top electrodes indicate a pseudo-ohmic behavior, and double humps in the second derivative of transconductance (dg_m) curves were clearly observed, manifesting conducting channel migration along the *c*-axis of WSe_2 multilayers as a function of drain bias (V_D) conditions. On the other hand, at the bottom electrodes displaying a relatively high contact resistance, the second hump of dg_m exclusively appeared at high V_D regimes ($3.0 \text{ V} \leq V_D$), signaling the restricted channel migration caused by poor contact quality, even in the identical WSe_2 multilayers. In addition, we confirmed this distinct feature in dg_m curves by connecting the bottom- and top-electrodes together to support our observation. Furthermore, a conventional low-frequency noise analysis was employed to determine the surface trap density of supporting dielectrics and the relevant carrier scattering mechanism. Our study provides deep insights into the effects of contact resistance on carrier transport in not only WSe_2 multilayer transistors but also other 2D multilayers, suggesting the way on the optimization of device performance and contact quality.

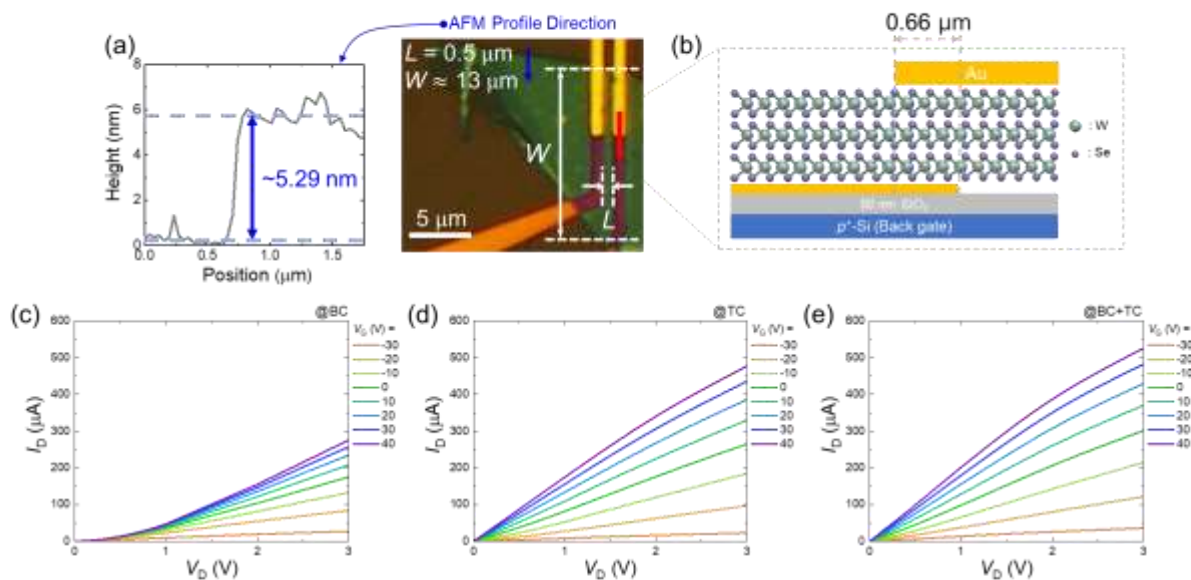

Figure 1. Device structure and schematic of WSe_2 field-effect transistors. (a) Optical image of our fabricated WSe_2 multilayer device on a 90-nm-thick SiO_2/p^+-Si wafer (right panel) Scale bar represents 5 μm. Thickness profile confirmed by AFM along the blue arrow (left panel). (b) Schematic diagram of 2D cross-sectional view at the red line of Fig. 1(a). Linear-scaled drain current-voltage output characteristic curves (I_D–V_D) obtained from (c) BC, (d) TC, and (e) BC+TC, respectively.