Hetero-integration of layered semimetallic electrodes for future CMOS devices

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Hetero-Integration of the emerging two dimensional (2D) layered materials with the existing CMOS platform is a viable solution to enhance the performance and functionalities of the future CMOS based integrated circuits. In this direction, we conducted experimental investigations to assess the applicability of 2D layered semimetals, specifically T_d-WTe_2, 1T'-$MoTe_2$, 1T-$PtTe_2$ and 1T-$PtSe_2$ as an electrode with two most commonly used semiconductors i.e. silicon and germanium prevalent in the CMOS technology. Two kinds of devices i.e. metal-oxide-semiconductor (MOS) capacitors and metal-semiconductor (MS) diodes are investigated with these semimetals as conducting electrode. Through detailed electrical and physical characterizations, it is established that these semimetals form excellent interface with the underneath dielectric (SiO_2) in the MOS structure and with the semiconductor (Ge) in the MS diodes. Near ideal CV curves of MOS devices and large ON current in the MS diodes signify that these semimetals perform well as a contacting electrode. The effective work function (WF) of semimetals is evaluated CV of the MOS devices. Reduction in the Schottky barrier height (SBH) in the MS diodes with decreasing values of the semimetal WF suggests the excellent interface of these semimetals with the germanium substrate. Most importantly, these semimetals do not add any unwanted series resistance across the current conduction path in both the MS diode and MOS capacitors. The high break down voltage of SiO_2 in MOS structure establishes that the transfer process of ultra-clean, dangling bond free semimetals does not introduce any defects and contaminations to the underneath dielectric which also have been confirmed with the HRTEM analysis. Guided by these experimental observations, we propose that these semimetals are CMOS friendly and can be integrated as an electrode with conventional silicon, germanium devices and with the atomically thin 2D semiconductor devices.

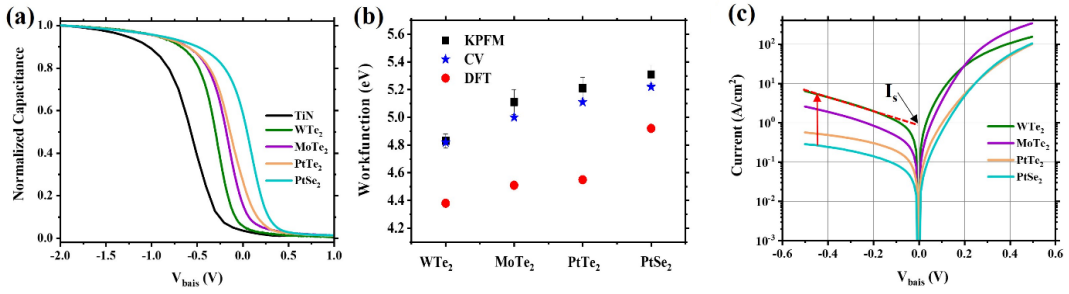

Figure 1. (a) The normalized CV curves of the MOS capacitors with layered semimetals and conventional 3D metal TiN as a gate electrode. (b) The WF of the semimetals evaluated using KPFM, MOS capacitors and DFT calculations. (c) The I-V curve of semimetal/n-Ge diodes, the red arrow shows the modulation of off current by changing the semimetal with different work function.

References

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