# Large room-temperature magnetoresistance in all-van der Waals magnetic tunnel junctions

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The magnetic tunnel junction (MTJ) is the core component in memory technologies, such as magnetic random-access memory, magnetic sensors and programmable logic devices. In particular, MTJs based on two-dimensional (2D) van der Waals (vdW) heterostructures offer unprecedented opportunities for low power consumption and miniaturization of spintronic devices. An ambitious vision has been proposed for all-vdW MTJ devices by Yang *et al.* in [1]. However, the operation of 2D MTJs at room temperature remains a challenge. Tunnel magnetoresistances (TMRs) in previous vdW-based junctions were only observed at low temperatures. For example, the $Fe_3GeTe_2$-based MTJ shows a TMR of 300% at $T$ = 4.2 K [2] but the TMR vanishes at around 220 K [3].

Here, we report a large TMR of up to 85% at room temperature ($T$ = 300 K) in vdW MTJs based on a thin (< 10 nm) $WSe_2$ semiconductor spacer layer embedded between two $Fe_3GaTe_2$ electrodes with intrinsic above- room temperature ferromagnetism (Figure 1) [4]. The room-temperature magnetoresistance is comparable to that of state-of-the-art conventional MTJs and represents a significant advance, opening a realistic and promising route for next-generation spintronic applications.

## References

[1] Yang, *et al.*, Nature, 606 (2022) 663
[2] Min, *et al.*, Nat. Mater., 21 (2022) 1144
[3] Fei, *et al.*, Nat. Mater., 17 (2018) 778
[4] Zhu, *et al.*, Chin. Phys. Lett., 39 (2022) 128501

## Figures

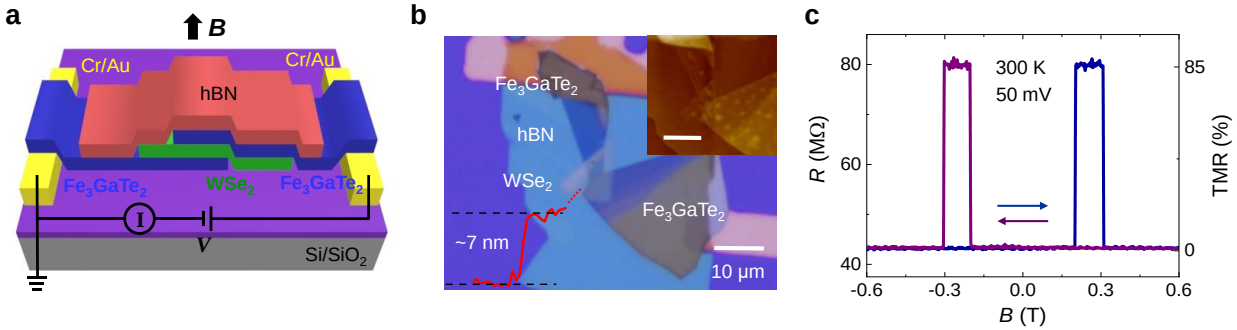


**Figure 1:** (a) Schematic of a $Fe_3GaTe_2/WSe_2/Fe_3GaTe_2$ MTJ. (b) Optical image and AFM image (upper-right inset) of a representative $Fe_3GaTe_2/WSe_2/Fe_3GaTe_2$ heterojunction device encapsulated by a top hBN layer. Scale bar: 10 μm. The lower-left inset shows the height profile of the spacer layer $WSe_2$. (c) Room-temperature resistance ($R$) and TMR versus perpendicular magnetic field ($B$) of the device at a constant bias voltage $V$ = 50 mV.