Performance, challenges, and reliability of 300mm FAB integrated 2D TMDCs based devices

César Javier Lockhart de la Rosa
Imec, Kapeldreef 75, 3001 Leuven
lockhart@imec.be

2D TMDCs have demonstrated to be rightful contenders as the material of choice for high performance logic devices. However, most of these demonstrations have been done, up to now, relying on lab-base integrated devices. In this talk I will start by covering the performance of devices and circuits integrated in a 300mm FAB [1]. Then I will proceed to put the spotlights on some of the challenges such an integration might represent for the industry. I will then follow with the solutions that we have found for some of them such as top contacting integration on 300mm scale [2] and 300mm FAB integrated devices using a 300mm compatible transfer of 2D materials [3].

I will then proceed to highlight the importance of the reliability of such devices and a first order analysis of the BTI impact on 2D TMDCs based 300mm FAB integrated devices [4] and the effect of the gate-stack oxide charge trapping on the performance of such devices [5].

Finally, I will motivate and challenge the community to commit to tackle further obstacles foreseen on the integration in a reliable and reproducible way of this materials on novel high performing devices architectures [6].

References

[1] T. Scram, SNW, 2022
[2] S. Kundu, VLSI, 2023
[3] S. Ghosh, VLSI, 2023
[4] L. Panarella, DRC, 2022
[5] L. Panarella, IRPS, 2022
[6] T. Schram, Adv. Mater., 2022, 34, 2109736