

Graphene-Integrated Steep-Slope Field-Effect Transistor

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The continuous down-scaling of MOSFETs has generated the urgent demand for steep-slope transistors with reduced sub-threshold swing (SS) and low power consumption [1-3]. In this work, single-layer graphene is integrated in the gate structure of a MoS₂ channel FET which led to a subthreshold swing as low as 31 mV/dec, well below the “fundamental” limit of 60mV/dec. Exploiting the negative electronic compressibility in single-layer graphene with low density of states, negative quantum capacitance was obtained within a certain gate voltage range. Similar to “traditional” negative capacitance obtained with ferroelectric materials, the negative quantum capacitance enables internal gate voltage amplification and subthreshold swing well below 60 mV/dec [4, 5]. Theoretical simulations reveal the fundamental mechanism which explains the negative quantum capacitance observed when a single-layer graphene is encapsulated (integrated) within the gate stack. The results point to a new pathway for the development high speed and low power transistor devices.

References

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Figures

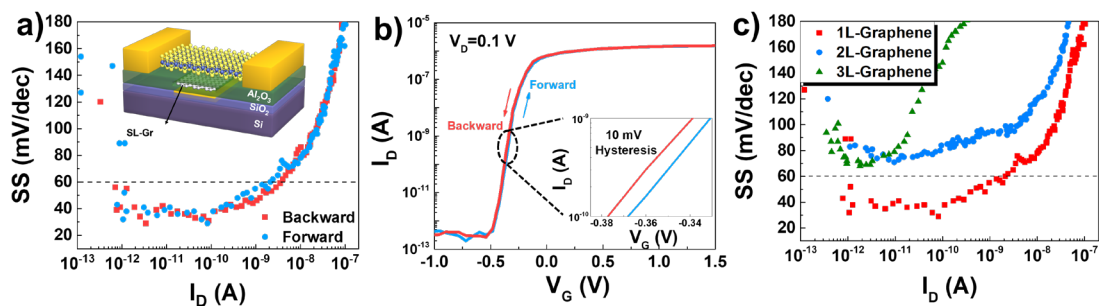


Figure 1: (a) SS values extracted from (b) ID-VG curves. (c) SS values of the device with different graphene layer thickness.

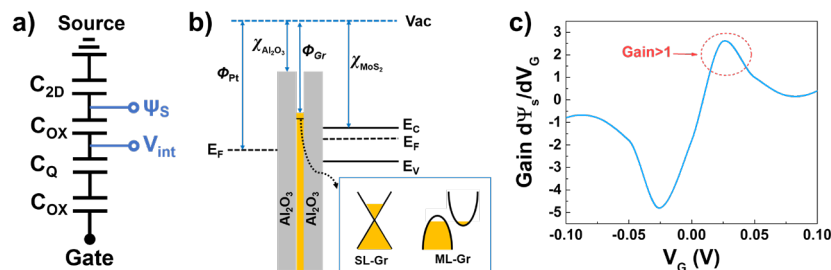


Figure 2: (a) Capacitor divider model and (b) band diagram of the gate stack. (c) Simulation results.