

Enhanced Top-gate Monolayer MoS₂ Transistor Using iCVD Based High-k Dielectric

SeoHak Park¹

SangHun Lee¹, Woonggi Hong¹, and Sung-Yool Choi^{1*}

¹School of Electrical Engineering, Graphene/2D Materials Research Center, Center for Advanced Materials Discovery towards 3D Displays, KAIST, 291 Daehakro Yuseong-gu, Daejeon 34141, South Korea.

psh851416@kaist.ac.kr

Abstract

Because of the dangling bond free nature of 2D-channel materials, 2D-materials based transistor shows incongruity with a conventional ALD dielectric deposition process. Especially 2D-materials based transistors generally show inferior characteristic when they are applied in a form of top gate transistor. [1] In this study, by applying a newly invented initiated chemical deposition (iCVD) process based high-k dielectric p(HEMA)-g-AlO_x as a top gate insulator of MoS₂ transistor, high performance top gate monolayer MoS₂ transistor with mobility of 12cm²V⁻¹s⁻¹, SS of 135mVdec⁻¹ with low hysteresis (<100mV) value is developed. [2] With systematic analyses, we could confirm that the reason for this improvement is due to a less coulombic scattering effect and a less surface optical phonon scattering effect of a hybrid dielectric based top-gate MoS₂ transistor than those of Al₂O₃ dielectric based top-gate device.

References

[1] Subhamoy Ghatak et al., ACS Nano, 5 (2011) 7707-7712.

[2] L. Yu et al., IEDM, 32 (2015) 1-4.

Figures

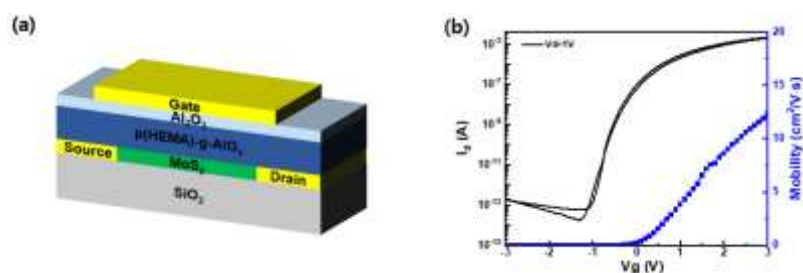


Figure 1: (a) Schematic illustration of fabricated device. (b) transfer characteristic of p(HEMA)-g-AlO_x/MoS₂ top-gate device.

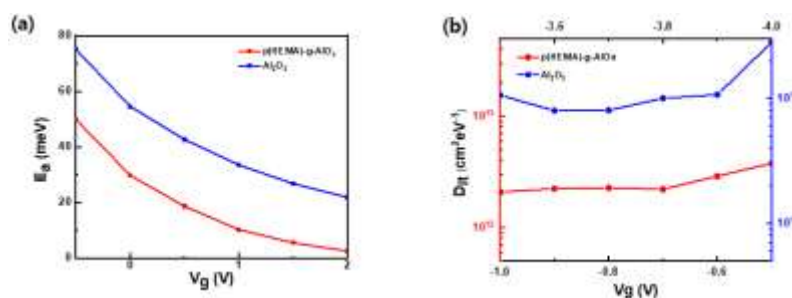


Figure 2: (a) Comparison of activation energy between Al₂O₃/MoS₂ top-gate device and p(HEMA)-g-AlO_x/MoS₂ top-gate device. (b) Difference of interface trap density (D_{it}) for each applied dielectric film.