

# Advancing 2D Monolayer CMOS Through Contact, Channel and Interface Engineering

---

## Kevin P. O'Brien

Chelsey D Dorow, Ashish Penumatcha, Kirby Maxey, Ande Kitamura, Susu Lee, Carl H. Naylor, C. Rogan, D. Adams, T. Tronic, T. Zhong, A. Oni, A. Sen Gupta, R. Bristol, S. Clendenning, M. Metz, U. Avci

Components Research, Intel Corporation, Hillsboro, OR 97214, USA.

[kevin.p.obrien@intel.com](mailto:kevin.p.obrien@intel.com)

---

## Abstract

2D CMOS transistors fabricated with transition metal dichalcogenide (TMD) materials are a potential replacement for silicon transistors at sub-12 nm channel length [ $L_G$ ]. [1],[2],[3]. Here we present progress towards the ultimate goal and outline critical research needs. We share a design choice that theoretically beats Silicon and saves significant switching energy. We demonstrate record NMOS contacts using a high melting point metal, down to 146  $\Omega\text{-}\mu\text{m}$  contact resistance ( $R_C$ ). We present the best PMOS performance on a grown monolayer WSe<sub>2</sub> film with 100  $\mu\text{A}/\mu\text{m}$  Ion and low sub-threshold swing (SS) using a Ruthenium contact metal, showing record PMOS contact resistance,  $R_C = 2.7 \text{ k}\Omega\text{-}\mu\text{m}$ . We present 300 mm wafer growth options of 4 different 2D TMD films: MoS<sub>2</sub>, WS<sub>2</sub>, WSe<sub>2</sub>, MoSe<sub>2</sub> grown at BEOL temperatures. Finally, we benchmark our results against leading TMD devices, while arguing for more directed research in the pmos device area.

## References

---

- [1] K.P. O'Brien, C.D. Dorow et al, IEDM 2021
- [2] C.D. Dorow, K.P. O'Brien et al VLSI 2021
- [3] K. Maxey et al VLSI 2022