# Opto-Electronic Modulation of the Monolithically Integrated Ferroelectric-Semiconductor Heterojunction for Multibit Memory devices

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In recent years, ferroelectric-semiconductor (FS) heterojunctions are drawn massive interest in the field of multifunctional nanoelectronics, such as phototransistor, memory, data processing, neuromorphic computing etc.[1] Furthermore, the stable remnant polarization with unique in-plane (IP) and out-of-plane (OOP) dipole coupling down to the monolayer limit (~1.2 nm) in $In_2Se_3$ becomes the central attention of ferroelectric research interest.[2] The strong light-sensitivity towards visible-to-near-infrared illumination also making it attractive for photoactive applications. Herein, we demonstrated a scalable and site-specific direct writing approach on few-layers of indium selenide ($In_2Se_3$) to create the $In_2Se_3$-$In_2O_3$ coplanar heterojunction using scanning visible-laser probe. The locally converted region was thoroughly characterized by in-depth microscopic (HRTEM, AFM and KPFM) and spectroscopic (Raman, PL and ToF-SIMS) means to understand the conversion dynamics.[3] Furthermore, the fabricated planar heterojunction has been utilized as self-powered broadband photodetector by using the built-in interfacial potential along with the ferroelectric field in $In_2Se_3$. The heterojunction exhibits superior photoresponsivity (857 A/W) without any external bias.[3] In addition, the ferroelectric polarization states in α-$In_2Se_3$ are utilized to control the device characteristics and thereby used to realize non-volatile memory (NVM).[4] The state-of-art multibit logic device was demonstrated by utilizing the polarization directions dependent (opto-)electronic output currents. The presented process enables a promising technological prospect to make all 2D lateral heterojunctions construction and could provide a platform for realizing wafer-scale integration of nanoscale devices with multiple advanced functionalities.

## References

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[3] S. Mukherjee D. Dutta, P.K. Mohapatra, L. Dezanashvili, A. Ismach and E. Koren, ACS Nano, 14 (2020), 17543–17553.
[4] D. Dutta, S. Mukherjee, M. Uzhansky and E. Koren, npj 2D Mater. Appl., 5 (2021), 81.

## Figures

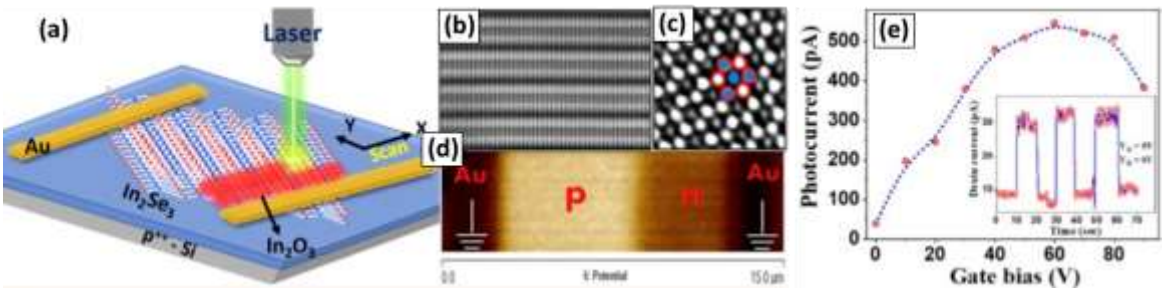


**Figure 1:** (a) Schematic illustration of the heterojunction fabrication using scanning laser microscopy. High-resolution (HR) TEM micrographs of $In_2Se_3$ in (b) cross-section-view and (c) top-view mode. (d) Surface potential mapping of the heterojunction FET channel, for equilibrium condition, which depicted the respective fermi-level alignment in the device. (e) Photocurrent variation as a function of gate bias. Inset shows the temporal time response in zero-bias condition.