Modular compact modelling technology for the simulation of integrated circuits based on graphene field-effect transistors

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Abstract

We report on the progress made towards the definition of a modular compact modeling technology for graphene field-effect transistors (GFET) enabling the electrical analysis of arbitrary GFET-based integrated circuits [1-5]. A set of primary models embracing the main physical principles defines the ideal GFET response under DC, transient (time domain), AC (frequency domain), and noise analysis (Fig. 1). Other set of secondary models accounts for the GFET non-idealities such as extrinsic-, short-channel-, trapping/detrapping-, self-heating-, and non-quasi static- effects, which could have a significant impact under static and/or dynamic operation. At both device and circuit levels, significant consistency between the simulation output and experimental data for relevant operating conditions is demonstrated. We also provide a perspective of the challenges ahead to scale up the GFET modeling technology towards higher Technology Readiness Levels while drawing a collaborative scenario among fabrication technology groups, modeling groups and circuit designers.

References

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Figures



Figure 1: The realization of a compact modeling technology for the simulation of graphene based integrated circuits requires the development of a set of models capturing the relevant physical effects for each type of circuit analysis: DC, transient (time domain), AC (frequency domain), noise. The primary models describing the ideal device are framed by black solid lines, while the secondary models describing the device non-idealities are framed by black dashed lines. Acronyms used - SHE: self-heating, SCE: short-channel effects, QS: quasi-static, NQS: non-quasi-static, MF: medium frequency, HF: high frequency, LFN: low-frequency noise, HFN: high-frequency noise.

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