Scalable Two-Dimensional Semiconductors for Electronics and Photonics

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Abstract

The isolation of a growing number of two-dimensional (2D) materials has inspired worldwide efforts to integrate distinct 2D materials into van der Waals (vdW) heterostructures. While a tremendous amount of research activity has occurred in assembling disparate 2D materials into "all-2D" van der Waals heterostructures and making outstanding progress on fundamental studies, practical applications of 2D materials will require a broader integration strategy. I will present our ongoing and recent work on integration of 2D materials with 3D electronic materials to realize logic switches and memory devices with novel functionality that can potentially augment the performance and functionality of Silicon technology. First, I will present our recent work on gate-tunable diode[1] and tunnel junction devices[2] based on integration of 2D chalcogenides with Si and GaN. Following this I will present our recent work on non-volatile memories based on Ferroelectric Field Effect Transistors (FE-FETs) made using a heterostructure of MoS_2/AlScN[3, 4] and I also will present our work on Ferroelectric Diode devices also based on thin AlScN.[5]

Next, I will present our work on light-trapping in excitonic systems[6] namely, 2D chalcogenides and halide perovskites. I will present the effect of nano-structuring on hybridization between excitons, plasmons and cavity photons.[7] I will extend this concept to artificial superlattice of 2D excitonic materials[8] as well as natural superlattices in the form of 2D halide perovskites[9] and demonstration of hybrid exciton-polariton emission at room temperatures.[10] If time permits, I will discuss our recent results on light trapping and giant linear dichroism in 2D antiferromagnetic semiconductors.[11] I will end by giving a broad perspective on future opportunities of 2D and other low-dimensional materials in basic science and applied microelectronics technology.

References

1. Miao, J.; et al. Jariwala, D., *Nano Letters* **2020,** *20* (4), 2907-2915.
2. Miao, J.; et al.Jariwala, D., *arXiv preprint arXiv:2111.06396* **2021**.
3. Liu, X.; et. al. Jariwala, D., *Nano Letters* **2021,** *21* (9), 3753-3761.
4. Kim, K.-H.; et al. Jariwala, D., *arXiv preprint arXiv:2201.02153* **2022**.
5. Liu, X.; et al. Jariwala, D., *Applied Physics Letters* **2021,** *118* (20), 202901.
6. Anantharaman, S. B.; Jo, K.; Jariwala, D., *ACS Nano* **2021**.
7. Zhang, H.; et al. Jariwala, D., *Nature Communications* **2020,** *11* (1), 3552.
8. Kumar, P.; et al. Jariwala, D., *Nature nanotechnology* **2022,** *17* 182–189.
9. Song, B.; et al. Jariwala, D., *ACS Materials Letters* **2021,** *3* (1), 148-159.
10. Anantharaman, S. B.; et al. Jariwala, D., *Nano Letters* **2021,** *21* (14), 6245-6252.
11. Zhang, H.; et al. Jariwala, D., *Nature Photonics* **2022,** *16*, 311-317.