Top Gate Length Dependence of Hysteresis in 300mm FAB MoS_2 FETs

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The use of MoS_2 as a channel in FETs can potentially enable outstanding scaling opportunities which are not accessible with Si [1]. Recently, imec has demonstrated the FAB line processing of top-gated WS_2 FETs on 300mm substrates [2]. We now present the integration of MoS_2 grown on sapphire and transferred to 300mm wafers (Figure 1a,b). These devices can exhibit promising performance with an on/off current ratio up to 10^4 when operated via the top gate (Figure 1c). However, their stability has not been studied so far. Here we have performed a detailed analysis of the hysteresis in these devices and found that it is typically more pronounced in FETs with larger top gate lengths L_{TG} (Figure 2a), as confirmed by the obtained statistics of the hysteresis width vs. reciprocal sweep time t_{sw} traces measured on multiple devices with L_{TG} between 70nm and 10µm (Figure 2b). However, our subsequent measurements at higher temperatures up to 175°C have revealed that for the shortest devices with L_{TG} = 70nm the hysteresis not just becomes smaller but also becomes counterclockwise at slow sweeps (Figures 2c,d). This suggests the involvement of thermally activated oxide traps situated close to the top gate electrode, which partially compensates standard charge trapping by border oxide traps situated close to the channel. Thus, we conclude that scaling of FAB MoS_2 FETs would require an in-depth study of charge trapping at both sides of the top gate insulator.

References

[1] S. Das et al., Nature Electronics, 4 (2021), 786.
[2] T. Schram et al., IEEE Symposium on VLSI Technology, pp. 1-2 (2021).

Figures

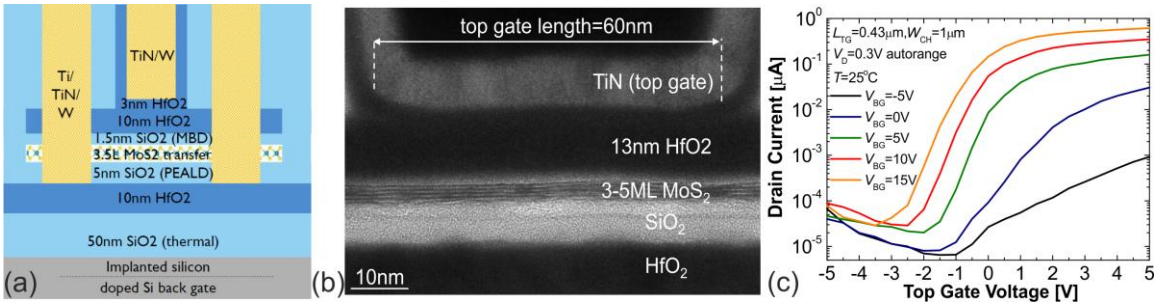

Figure 1: (a) Schematic layout of our FAB MoS_2 FETs. (b) TEM image of a device with L_{TG}=60nm. (c) I_D-V_{TG} curves of these devices vs. varied V_{BG}.

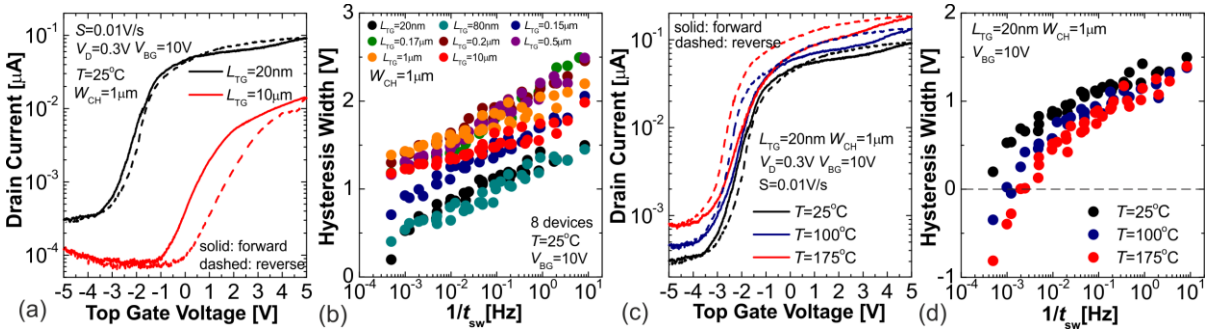

Figure 2: (a) Comparison of slow sweep I_D-V_{TG} curves for MoS_2 FETs with L_{TG} = 20nm and 10µm. (b) $\Delta V_H(1/t_{sw})$ traces for 8 devices with L_{TG} between 20nm and 10µm. (c) Slow sweep I_D-V_{TG} curves for the device with L_{TG} = 20nm measured at different temperatures. (d) The $\Delta V_H(1/t_{sw})$ traces show switching of the hysteresis towards the counterclockwise direction for slow sweeps and high temperatures.