Inkjet-printed low-dimensional materials-based complementary electronic circuits on paper

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At the dawn of the flexible and wearable electronics age, the seek for new materials enabling the integration of complementary metal-oxide-semiconductor (CMOS) technology on flexible substrates finds in low-dimensional materials (either 1D or 2D) extraordinary candidates. Together with their excellent electrical and mechanical properties, low-dimensional materials are solution processable and suitable to be cost-effectively deposited using high-throughput techniques, compatible with direct printing on different flexible substrates [1]. Here, we report an inkjet-printed CMOS-like technology on paper, combining *n*-type MoS_2-based and *p*-type carbon nanotubes (CNTs)-based field effect transistors (FETs) with hBN dielectric (Figure 1a). Both types of printed transistors exhibit good performances in terms of mobility (in the order of 10 cm^2/Vs) and ON/OFF current ratio (> 10^3), and their characteristics can be matched adjusting the channel dimensions (Figures 1b, c) [2]. The proposed devices have been successfully used to design and fabricate some fundamental CMOS building block, such as low-voltage inverters (Figure 2a), NOR gates (Figure 2b) and D-latches (Figure 2c), showing a path for the fabrication of efficient CMOS circuits for cost-effective applications.

References

[1] F. Bonaccorso et al., Advanced Materials vol. 28 (2016), 6136-6166
[2] I. Brunetti et al., npj 2D Materials and Applications vol. 5, (2021), 85.

Figures

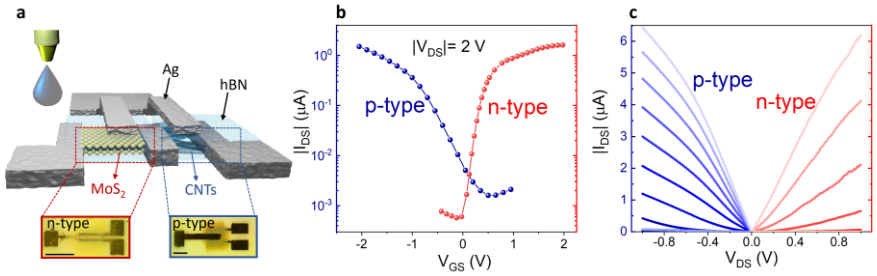

Figure 1: a) Sketch of the proposed CMOS-like circuit, together with the input (b) and output (c) characteristics of a p-type and a n-type FET.

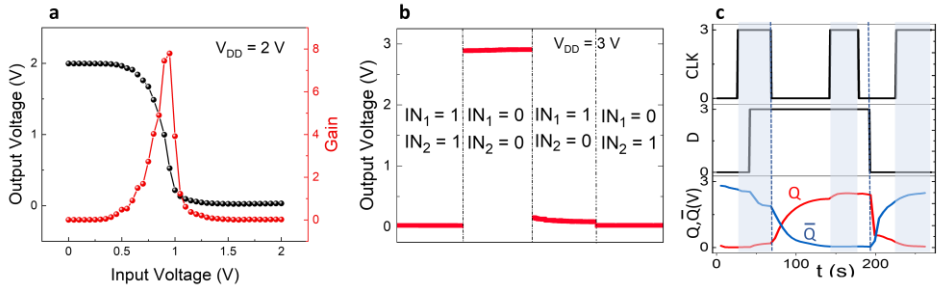

Figure 2: a) Input-Output characteristic (left axis) and voltage gain (right axis) of an inverter. b) Output voltage of a NOR gate as a function of the input states. c) Time evolution of the output, Q and /Q, as a function of the input signal, D, and clock, CLK.