Nonvolatile Memory Devices Utilizing $WSe_2/MoTe_2$ Stack Channel for Synaptic Device Operation

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Abstract

Nowadays, stacked two-dimensional materials receive high attentions, especially their van der Waals interaction at their stack junction interface. In this study, we report field effect transistors (FETs) with stacked transition metal dichalcogenide (TMD) channels, where the heterojunction interface between two TMDs appears useful for nonvolatile or neuromorphic memory FETs. Using patterned gate electrode and Al_2O_3 as gate dielectric, PS-brush treatment was conducted for minimize unwanted interface charge traps.[1] A few nm thin $MoTe_2$ and WSe_2 flakes are transferred on gate dielectric sequentially making vertical stack. We also conducted air ambient annealing at 200 ˚C to make $MoTe_2$ and WSe_2 p-type using MoO_x and WO_x, as WSe_2 and $MoTe_2$ are known for ambipolar materials. These interesting p-type/p-type semiconductor stack interface functions as hole trapping sites where traps behave nonvolatile although trapping/de-trapping can be controlled by gate voltage (V_{GS}). $WSe_2/MoTe_2$ stack device shows memory retention after high V_{GS} pulse appears longer than 10,000 s and Program/Erase ratio in drain current is higher than 200. Moreover, the traps are delicately controllable even with small V_{GS}, which indicates that a neuromorphic memory is also possible with our heterojunction stack FETs. Our stack channel FET demonstrates neuromorphic memory behavior of ~94% recognition accuracy.

References

[1] Y. Jeong, J. H. Park, J. Ahn, J. Y. Lim, E. Kim, S. Im. Adv. Mater. Interfaces. 5 (2018), 1800812

Figures

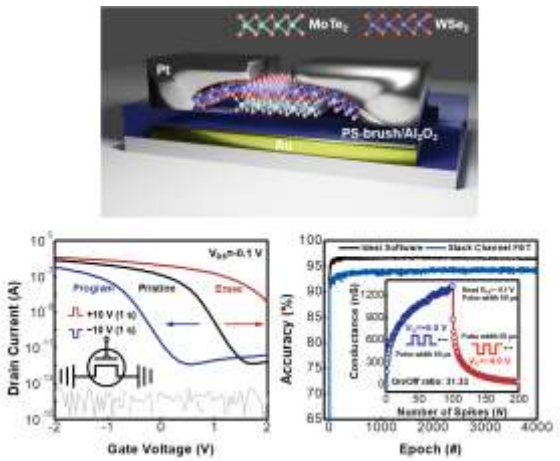

Figure 1: 3D schematic of the device with transfer characteristic and neuromorphic simulation.