The perspectives of 2D material growth in the future BEOL and FEOL technologies

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The increasing interest of 2D materials in the IC industry is key to bring these systems to wafer scale production. Their unique intrinsic properties at very low thicknesses offer new opportunities that bulk materials won't be able to meet at scaled dimensions and especially for the sub-10nm technological nodes [1]. In a 2D-based heterostructure, layers interact by vdW forces between each other. This would offer a promise to defect-free interfaces and thus better device performance. However, the big challenge remains in synthesizing these very thin layers on a 300 mm Si-wafer level. Problems of layer homogeneity, thickness control and defect engineering are of crucial importance for each application.

In this work, we start by giving an overview of some of the applications where 2D materials are expected to play an important impact. We will specifically talk how 2D materials can help in a) decreasing the RC delay of metal interconnects at the BEOL level and b) improve power switching in scaled transistors at the FEOL level. The focus will be then shed on the integration difference in each case. We emphasize on how the role of the growth temperature is affecting the material quality and the integration solution strategies (see figure 1). Lastly, we try to address the impact of defects on each application. These proposals could be extended for different kind of applications which can push forward the 2D integration in CMOS technology at both BEOL and FEOL levels.

References

[1] R Quhe et al. Physics Reports, (2021) ISSN 0370-1573, https://doi.org/10.1016/j.physrep.2021.07.006

Figures

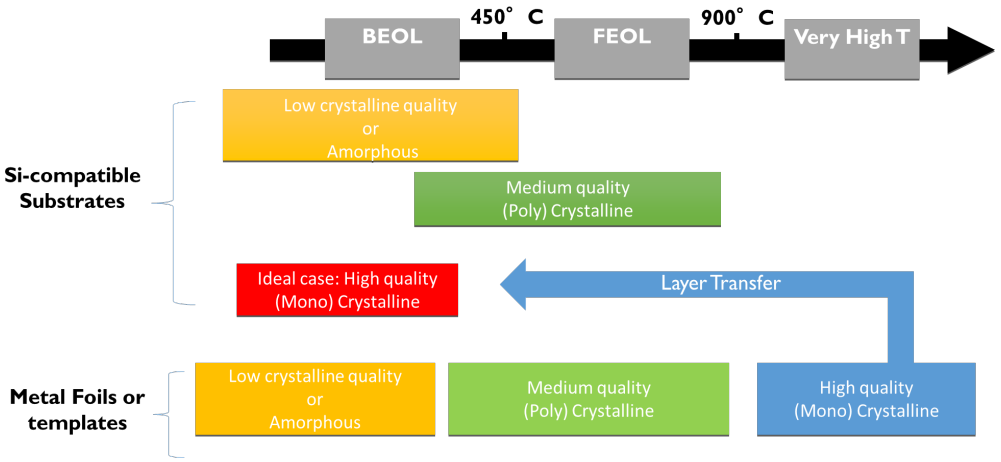

Figure 1: A summary illustration of the expected 2D material quality in function of the growth temperature on different type of surfaces. To achieve an ideal crystalline quality of 2D layer on Si substrates, a layer transfer seems to be essential. Efforts on removing this step can be a significant breakthrough in some applications where direct 2D monolithic integration on Si is a must.