## Superconducting contacts to mono- and few-layer semiconductor crystals

**Ian Correa Sampaio**<sup>[a]</sup>, Mehdi Ramezani<sup>[a,b]</sup>, Kenji Watanabe<sup>[c]</sup>, Takashi Taniguchi<sup>[c]</sup>, Zakhar R. Kudrynskyi<sup>[d]</sup>, Amalia Patanè<sup>[d]</sup>, Christian Schönenberger<sup>[a,b]</sup> and Andreas Baumgartner<sup>[a,b]</sup>

[a] Department of Physics, University of Basel, CH-4056, Basel, Switzerland

[b] Swiss Nanoscience Institute, University of Basel, CH-4056, Basel, Switzerland

[c] Research Center for Functional Materials, National Institute for Material Science, Tsukuba 305-0044, Japan

[d] School of Physics and Astronomy, University of Nottingham, NG7 2RD Nottingham, United Kingdom

ian.correasampaio@unibas.ch

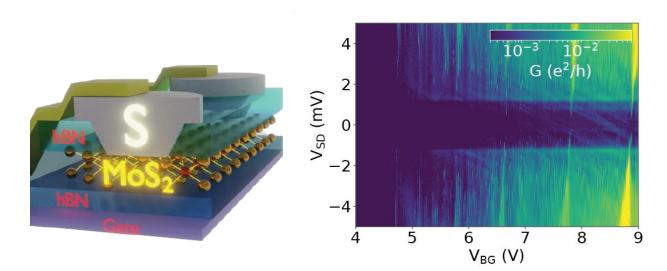
## Abstract

Superconductor-Semiconductor hybrid devices have proven most fruitful for fundamental research and applications, such as gate tunable qubits [1], thermoelectrics [2] and exotic quantum states [3]. Two-dimensional materials, such as transition metal dichalcogenides (TMDCs), are promising candidates for spin- and valleytronics applications, as well as a platform to study topological phenomena. Here, we demonstrate hybrid devices based on monolayer  $MoS_2$ , a semiconducting TMDC, contacted by vertical interconnect access (VIA) [4] superconducting contacts [5]. The transport characteristics of the devices exhibit a superconducting energy gap, which we probe as a function of magnetic field and temperature [5]. In addition, we discuss zerobias and finite-bias conductance peaks and Fabry-Pérot-type resonances, and compare  $MoS_2$  and InSe devices fabricated with the same method.

## References

- [1] T. Larsen et al., Phys. Rev. Lett. 115, 127001 (2015).
- [2] M. Leivo et al., Appl. Phys Lett. 68, 1996 (1996).
- [3] V. Mourik et al., Science, 336, 1003 (2012).
- [4] E. J. Telford et al., Nano Lett., 18, 1416 (2018).
- [5] M. Ramezani et al., Nano Lett., 21, 5614 (2021).

## Figures



**Figure 1:** Left: Illustration of superconducting VIA contacts in an MoS<sub>2</sub> device. Right: Differential conductance between two VIA contacts to a monolayer of MoS<sub>2</sub> plotted as function of the applied bias and gate voltage.