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EVALUATION OF GRAPHENE FET MODEL IN QUASI-BALLISTIC REGIME FOR FREQUENCY DOUBLER CIRCUIT

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***Abstract*—This paper, we present a radio frequency (RF) performance benchmarking for circuit design using the quasi-ballistic transport model of graphene FET (GFET) device as reported in earlier literature. The main objective of this work is to test the validity of reported model for RF circuit application. To this purpose, we have implemented the set of expression of GFET device in Verilog-A using circuit simulator like Cadence Virtuoso. Especially, we have simulated a GFET based frequency doubler circuits, which takes the advantage of the ambipolar conduction of graphene material.**

Keywords— Graphene FET, Verilog-A, quasi-ballistic, frequency doubler.

IV. RESULTS AND DISCUSSION

The Fig. 2(a) portrays the scattering mechanism among the channel charge carriers in terms of the backscattering coefficient (R) with respect to the drain-to-source voltage, for two channel lengths ($140,300\,nm$) of GFET device. From Fig. 2(a), it has observed that the charge carriers have more scattering among them for smaller values of V_{DS}. However, at higher values of V_{DS}, the charge carriers encounter less scattering among them and they are more directed, which results the lower value of the backscattering coefficient. Furthermore, the Fig. 2(b) demonstrates the variation of channel carrier concentration, from source side to drain end for two different channel lengths. From Fig. 2(b), it is observed that the GFET device with gate length $L = 140\,nm$, the *Dirac* point is closer to the source side, if we compare with the device having gate length $L = 300\,nm$. This is because, for smaller channel length, gate to source voltage has less control over the channel charge carriers and V_{DS} strongly influences the channel potential [5]. The $I_{DS} - V_{DS}$ characteristics of GFET for two different channel length ($L = 140,300\,nm$) are shown in Fig. 2(c) and 2(d) respectively. The kink-effect has observed, at $V_{T,GS} = -0.5\,V$, describes the ambipolar conduction in GFET device. The ambipolar conduction has three different regions of conduction viz., linear/triode, unipolar saturation, and ambipolar saturation. The linear and unipolar conduction of GFETs are look like same as in the conventional materials based MOS devices. However, in ambipolar conduction region, I_{DS} increases with V_{DS}. In ambipolar conduction region, the polarity of charge carriers near drain end are different comparing to the polarity of charge carriers near the source end of GFET devices.

This circuit shown in Fig. 4(a), capable to generate a signal at output terminal whose frequency is double that of the frequency of signal applied at input terminal. Herein, $R = 1K\Omega$ is a load resistor connected to the drain terminal of GFET. The quasi-ballistic compact analytical model [1], [2], has implemented in Verilog-A to create the sematic of GFET, which is further used to design and simulate the frequency doubler circuit. A dc gate voltage $0.37V$, input signal of frequency $1\,KHz$ and amplitude $300mV$ is applied at input of the circuit. The operation of the frequency doubler circuit is such that during the positive cycle of the ac input signal, GFET acts as an n-type MOS transistor and carrier conduction has take place in the channel from ground terminal (GND) to V_{DD}. However, in the negative cycle of input signal, the transistor then becomes p-type MOS device, and conduction of holes are from V_{DD} to the GND.

Table 1: List of Parameters are used in Simulation of GFET device taken from [12]

Parameters	Units	Values[12]
Length(L)	nm	140, 300
Width(W)	µm	1
Top gate oxide thickness (t_{ox})	nm	10
Temprature(T)	k	300
Fermi velocity(v_f)	m/s	$2.7x10^6$

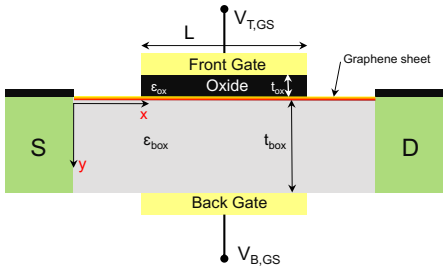

Fig.1 The cross-sectional view of modeled top gated Graphene FET device.

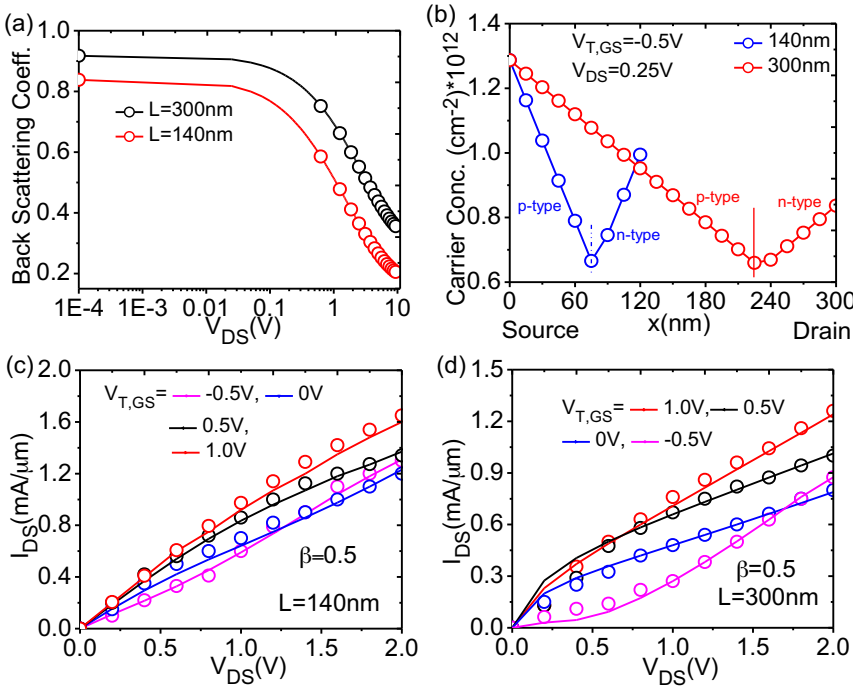

Fig. 2 (a) Backscattering coefficient (R) versus drain-to-source voltage (V_{DS}) for channel length $L = 300$ and $140\,nm$. (b) Carrier concentration along the channel length of top gate GFET for different values for channel length $L = 330$ and $140\,nm$. (c) Output characteristics of GFET device for $L = 140nm$, (d) for $L = 140nm$

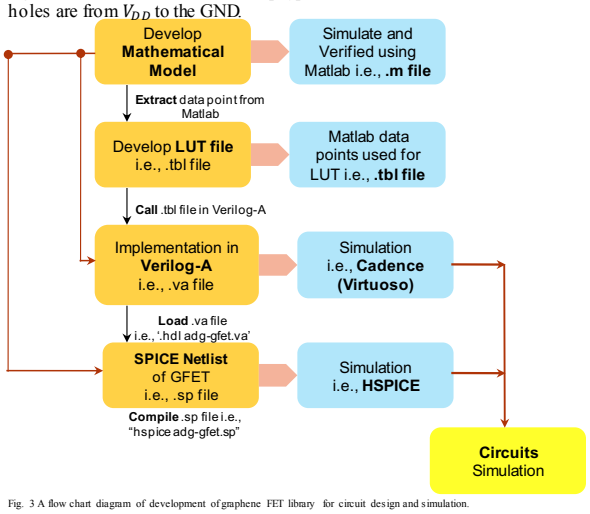

Fig. 3 A flow chart diagram of development of graphene FET library for circuit design and simulation.

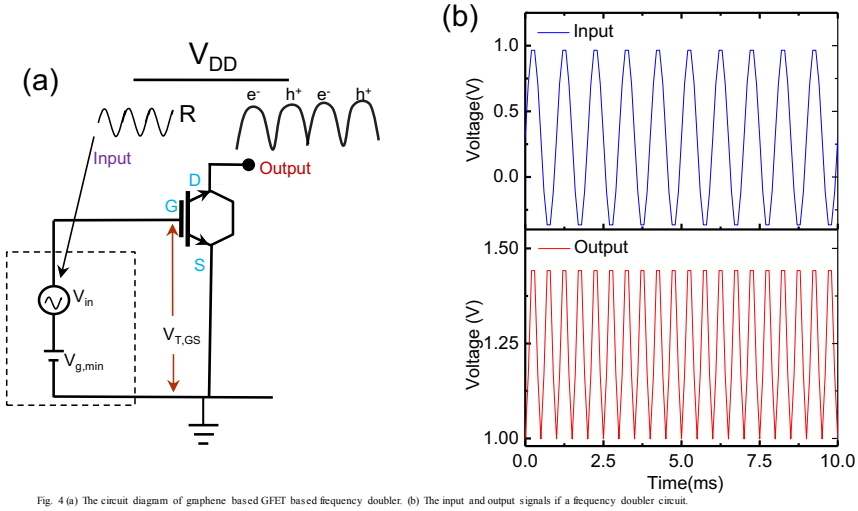

Fig. 4 (a) The circuit diagram of graphene based GFET based frequency doubler. (b) The input and output signals if a frequency doubler circuit.

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