Graphene field effect transistors using TiO_2 as the dielectric layer

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INTRODUCTION

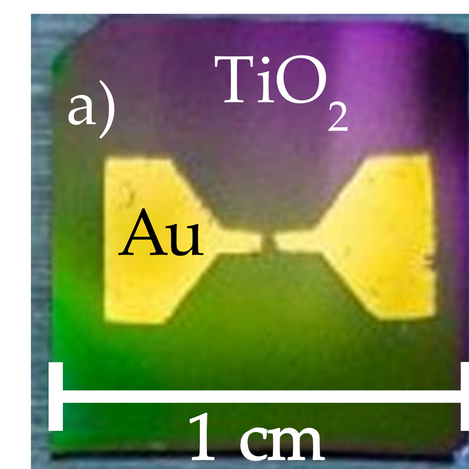
Graphene based electronic devices face the challenge to find a suitable dielectric material which has little or negligible effect in diminishing graphene's interesting properties, such as its electron and hole mobilities and its ambipolar effect. This work [1] explores the effect of TiO_2 as the dielectric layer on graphene field effect transistor's (GFETs) mentioned properties. Also we investigated the importance of the size and roughness of the graphene channel for these properties.

GOALS

1. Determine the Dirac voltage V_D, intrinsic charge carrier density n_0, and electron/hole mobilities $\mu_{e/h}$ for the fabricated GFETs.
2. Compare these devices with similar GFETs using SiO_2 as the dielectric layer.
3. Explore the effect that size and roughness of the graphene channel has on the electron/hole mobility.

GFETs FABRICATION

- 282 nm of TiO_2 were deposited via RF Sputtering onto Si doped substrates.
- Electrodes Drain and Source consisting of 150 nm of Au above 10 nm of Cr were deposited with the desired shape. (See Fig. 1-a).
- The channel area was designed to be 300x300 μm^2 between electrodes.
- Roughness of the TiO_2 layer was determined over the channel region using a profilometer.
- Graphene was synthesized via CVD method on copper foils and was transferred to the channel region by fishing it manually. (See Fig. 1-b).



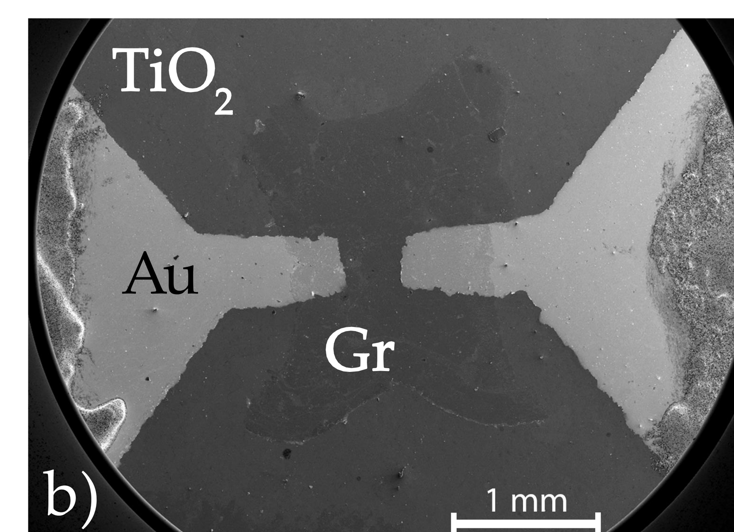


Figure 1. a) Photograph of the fabricated GFET. b) SEM image of the graphene transferred to channel region.

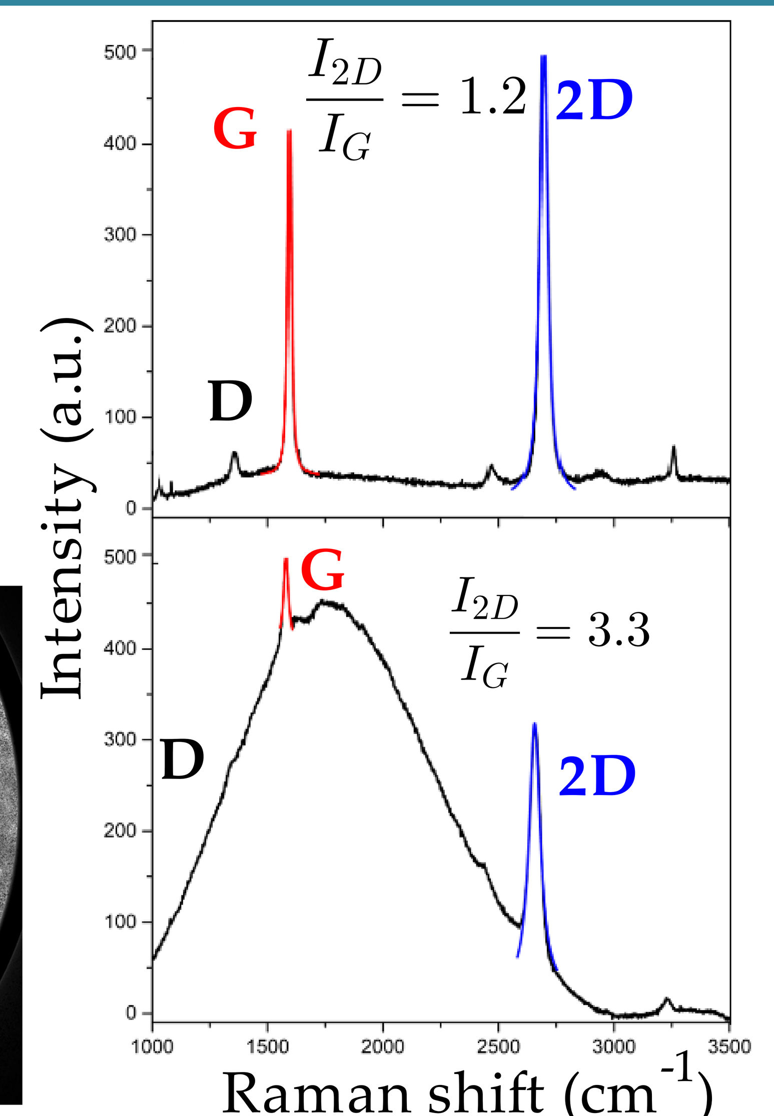


Figure 2. Raman spectra of graphene on Cu foil (below) and transferred onto TiO_2 (above).

MODEL & METHODOLOGY

- DC current sweep was driven between Drain-Source electrodes while measuring the V_{DS} voltage.
- Linear V_{DS} vs I_{DS} curves (graphene channel is ohmic).
- We fitted device's resistance to a model (Eq. 1) by Jia et al. [2]. Fitting parameters: R_x, n_0, $\mu_{e/h}$.

$$R_T = R_x + \frac{L}{We\mu\sqrt{n_0^2 + n^2}} \qquad (1)$$

$$n = \frac{C_g}{e}(V_g - V_D)$$

$$C_g = \frac{\varepsilon\varepsilon_0}{d}$$

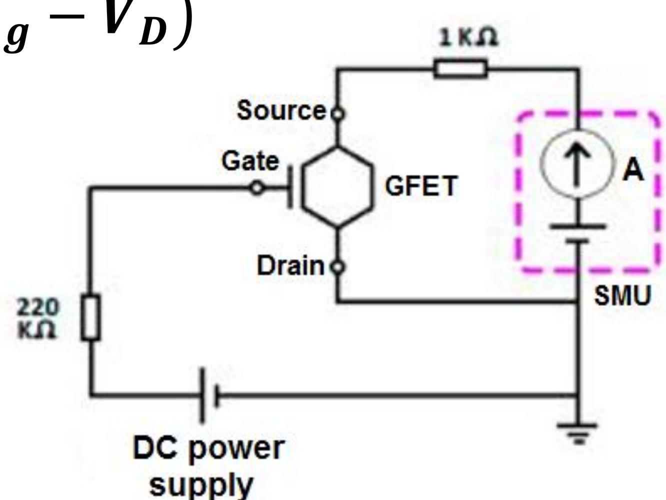


Figure 3. Circuit diagram.

RESULTS

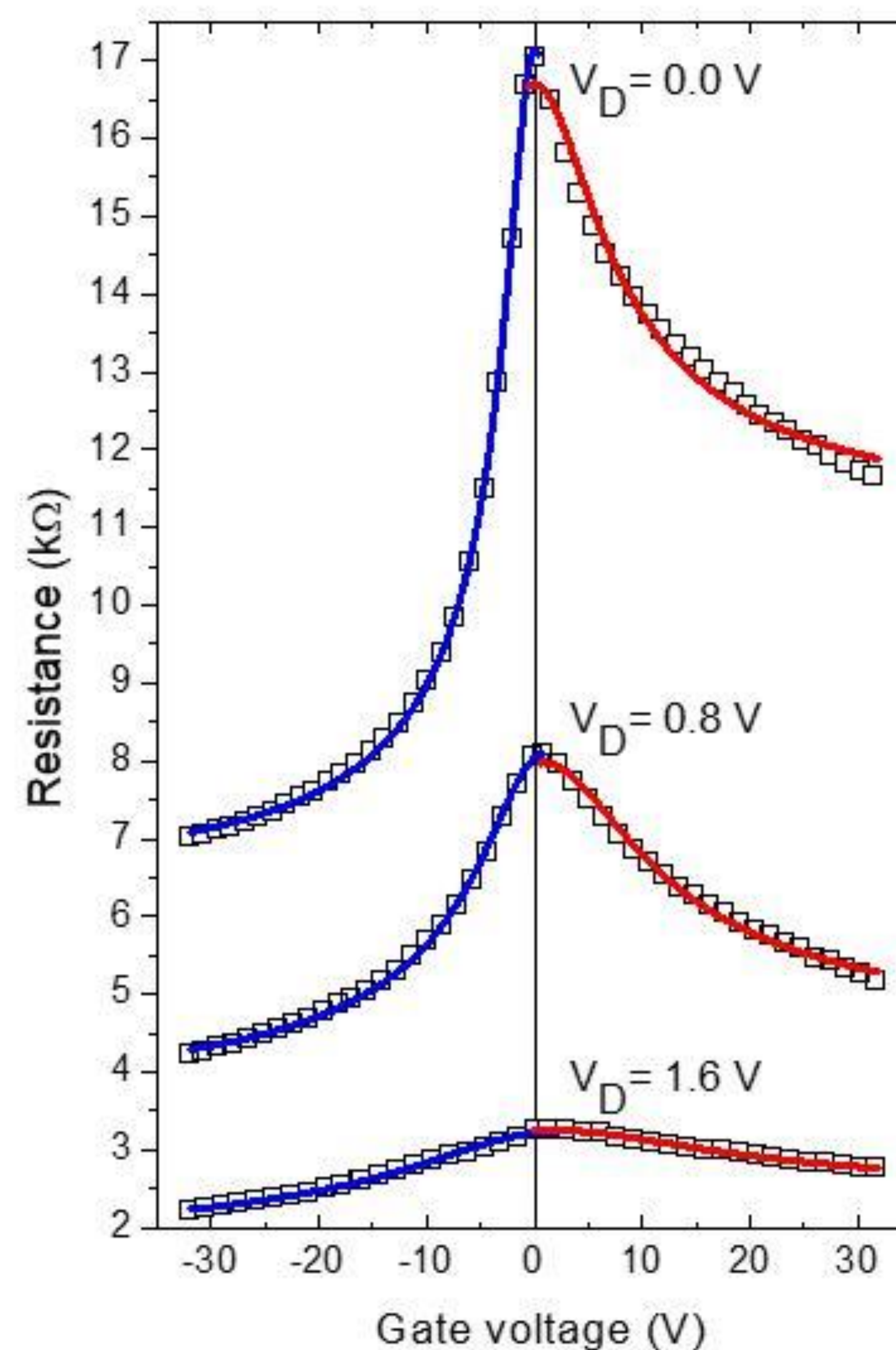


Figure 4. Measured resistance vs back gate voltage (squares). Fitted curve in colored lines.

Table 1
Table with electron and hole mobility and electron and hole carrier density for the three GFETs using $\varepsilon = 14$ for TiO_2[3].

GFETs' results			
Variables	GFET 1	GFET 2	GFET 3
V_D (V)	0	0.8	1.6
Silicon doping	n	n	p
R_x - holes (Ω)	6182 ± 6	3498 ± 6	1672 ± 12
R_x - electrons (Ω)	10868 ± 34	4336 ± 18	2406 ± 9
μ - holes (cm^2/Vs)	786 ± 2	865 ± 4	1120 ± 20
μ - electrons (cm^2/Vs)	688 ± 13	740 ± 10	1877 ± 46
n_0 - holes (1/cm^2)	7.25e11 ± 2e9	1.57e12 ± 1e10	3.58e12 ± 4e10
n_0 - electrons (1/cm^2)	1.55e12 ±3e10	2.32e12 ± 2e10	1.97e13 ± 1e11

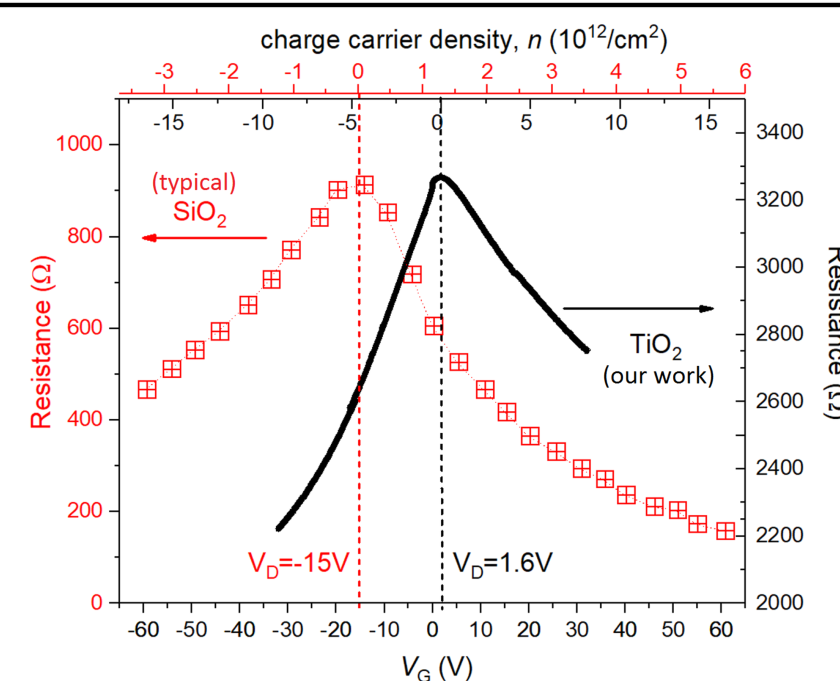


Figure 5. Comparison between our GFET 3and a typical SiO2 GFET [4].

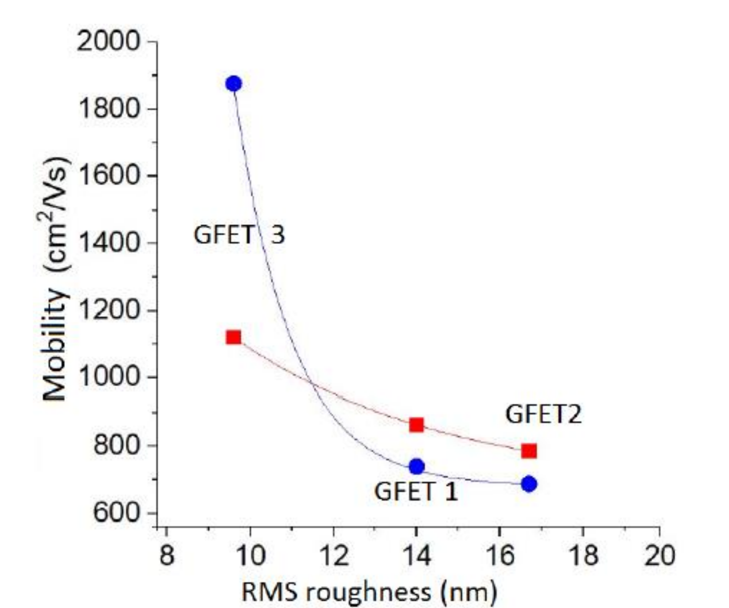


Figure 6. Electron (blue) and hole (red) mobilities vs the TiO2 roughness in the channel.

CONCLUSIONS

- We have obtained good mobility values up to 1877 cm^2/Vs, even tough the channel area is of hundreds of μm^2, knowing it conveys more defects.
- TiO_2 is a good material to combine with graphene for showing the ambipolar effect at very low voltages compared to SiO_2. See Fig. 5.
- The main difference between the fabricated GFETs was the roughness of the channel, which is a very important parameter to care about since it can decrease the mobility values as shown in Fig. 6.

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