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Optimal architecture for ultralow noise graphene transistors at room temperature

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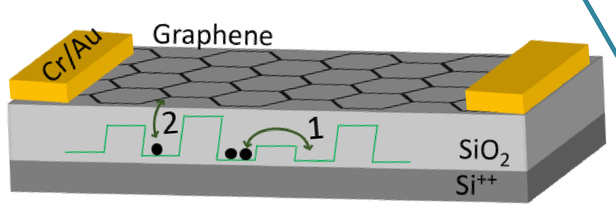
1. Motivation

❖ Dominant sources of 1/f noise in graphene FETs:

- **Mobility fluctuation (1)**: Hooge Model

$$\frac{S_V(f)}{V^2} = \frac{\gamma_H V^2}{nAf}$$

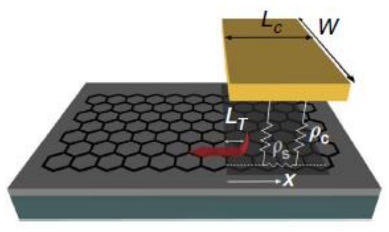


- **Charge density fluctuations (2)**: McWhorter Model

$$\frac{S_V(f)}{V^2} = \frac{6.2e^2K_B}{AkC^2f}\, TD_{it}\, \frac{g_m^2}{I_D^2}$$

- **Contact noise[2]**:

$$<(\Delta Rc)^2> \propto Rc^4$$

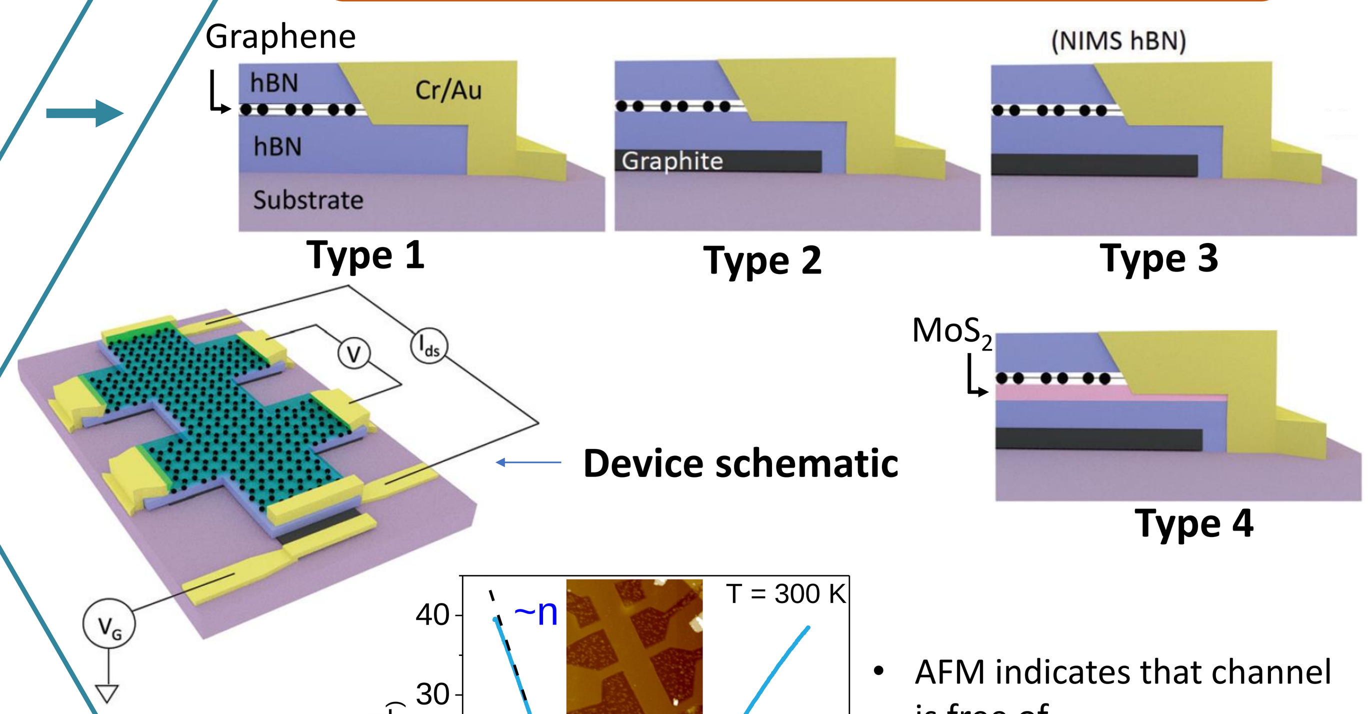


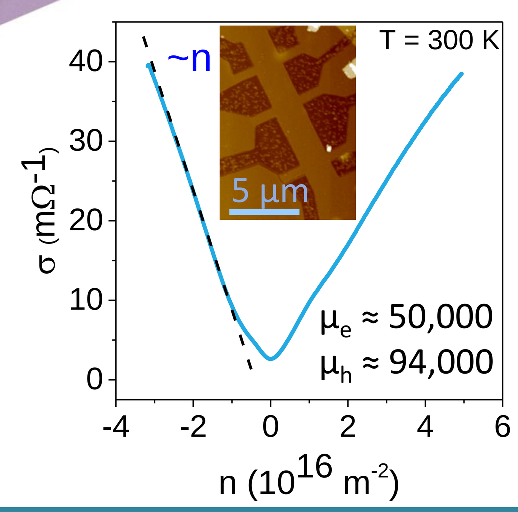
❖ Limited efforts exist to identify optimal architecture that minimizes noise in graphene FETs.

2. Introduction

- We study 1/f noise in graphene in various architectures to get ultralow noise graphene transistors.
- Noise not only limited to contact noise, but also to hBN trap states.
- MoS_2 underneath graphene further reduces the noise by screening the traps of hBN.
- Applications: high-sensitive sensors, optoelectronics, etc.

3. Various architectures and device characteristics

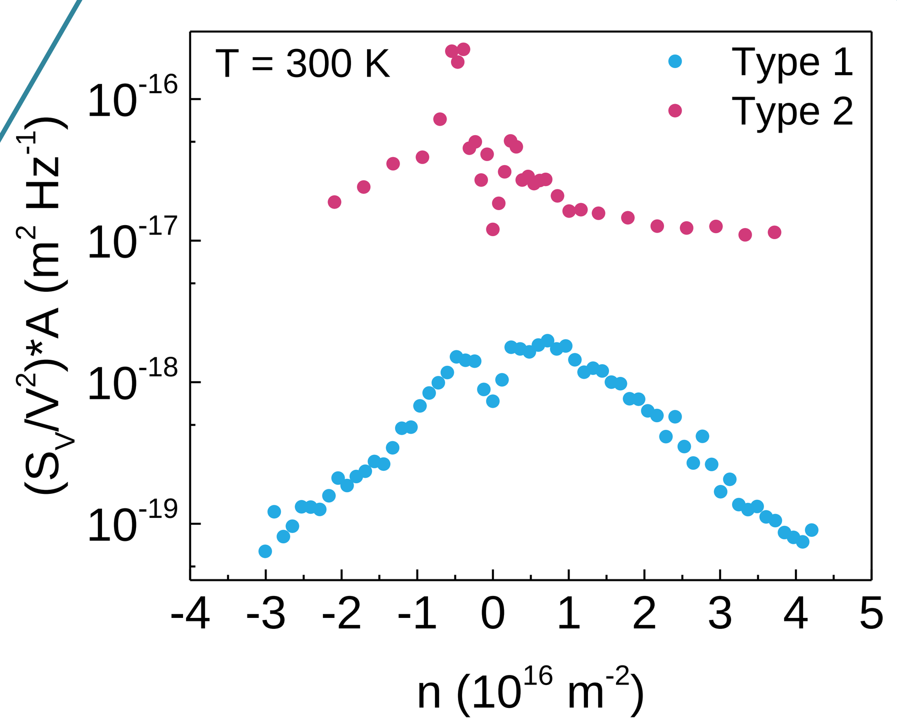




- AFM indicates that channel is free of bubbles/wrinkles/residues.
- Pristine channel of graphene reflects in mobility as well.

μ is in cm²/Vs

5. Graphite back gate

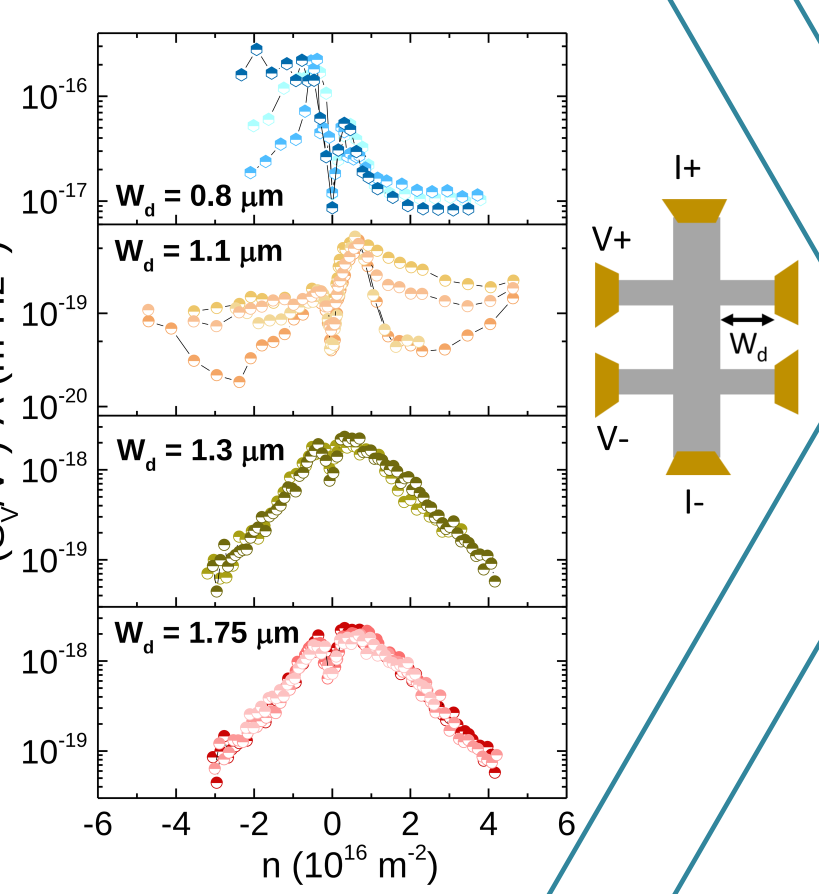


- Even on thick hBN, proximity effects of SiO_2 leads to fluctuations in graphene channel.
- Graphite back gate screens the potential fluctuations from SiO_2.

4. Contact noise elimination

- For $W_d < 1.2$ μm, contact noise dominates over channel noise.
- Non-local effects due to finite size of voltage probes can lead to fluctuations at the contacts.
- For $W_d > 1.2$ μm, normalized noise scales with area.
- Indicates, channel is the origin of noise.

W_d : Channel to contact distance



6. hBN traps

Normalised noise $\propto n^{-2}$

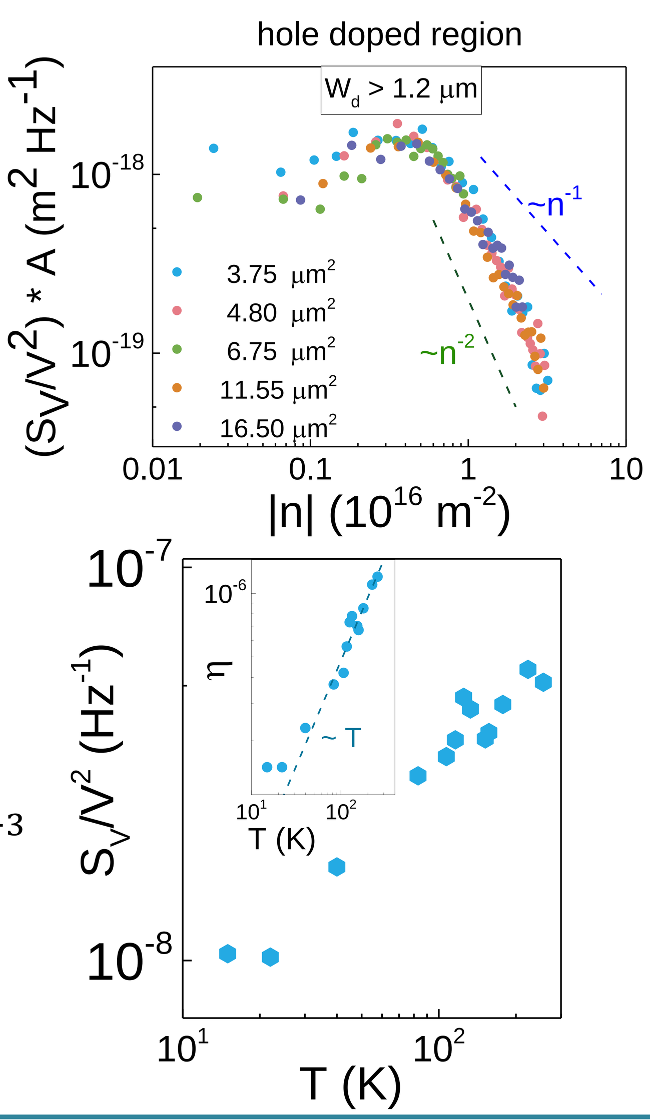
Implies, number density fluctuations.

$$\eta = \frac{\frac{S_V}{V^2}}{\frac{g_m^2}{I_D^2}}, \quad \eta = K * TD_{it}$$

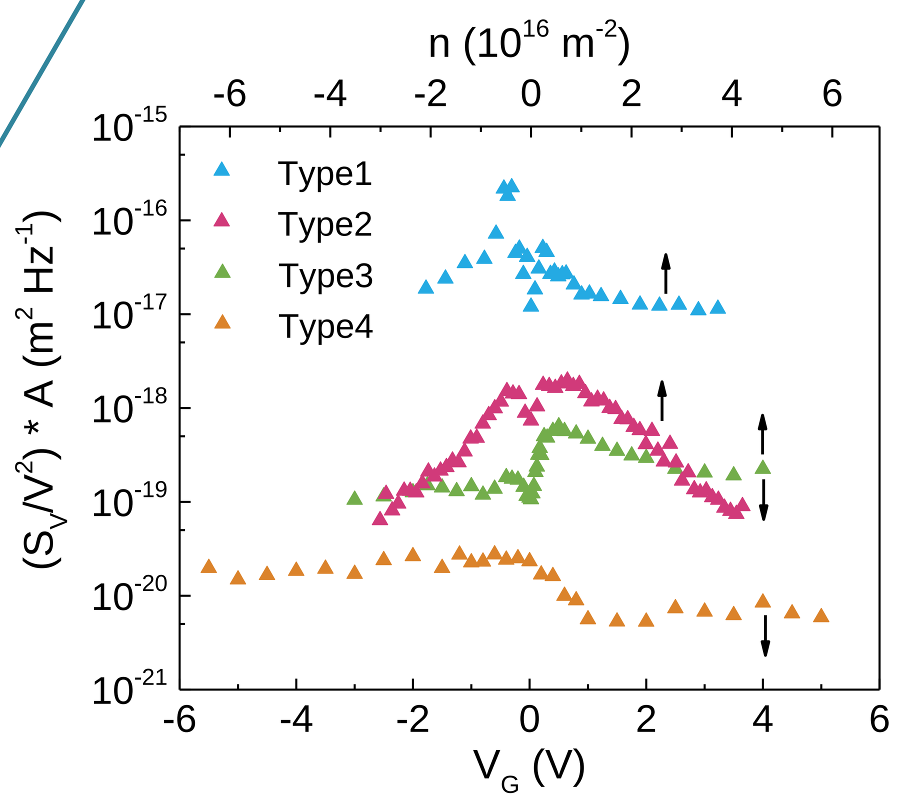
(Constant)

$$D_{it} \approx 2.7 * 10^{15}\, eV^{-1}cm^{-3}$$

Value of D_{it} agrees with reported trap density of hBN[3].

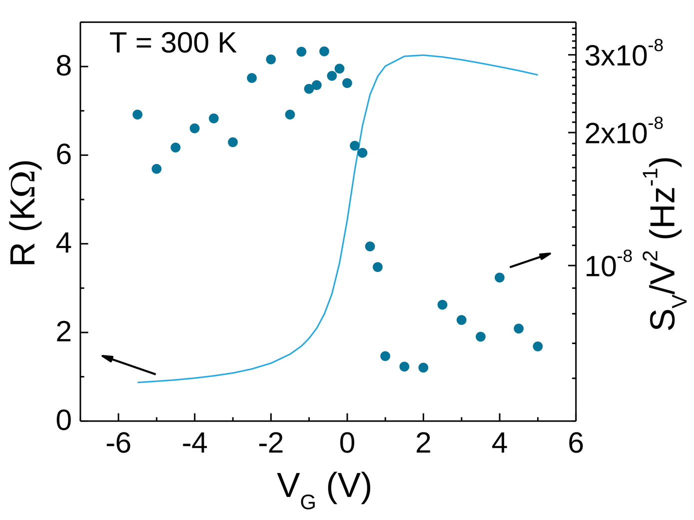


8. Optimal architecture



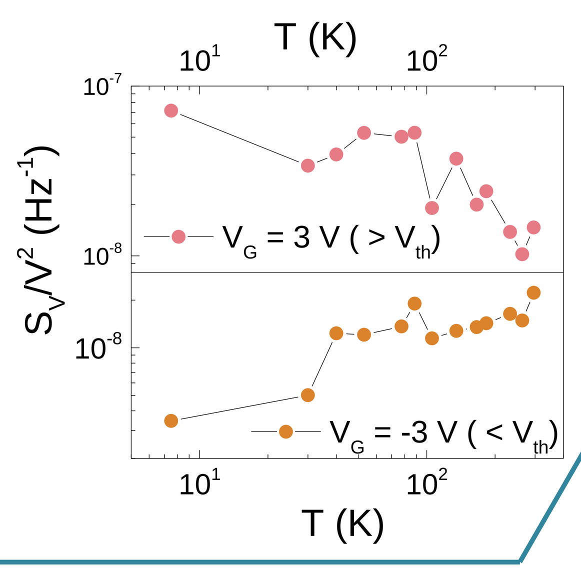
Type 4 architecture leads to lowest noise after removing contribution from contact noise and effects of fluctuations from bottom hBN traps.

7. MoS_2 as a screening layer



- As soon as MoS_2 is turning ON ($V_G > V_{th}$), noise reduces.
- MoS_2 is acting as a screening layer for fluctuations from hBN traps.

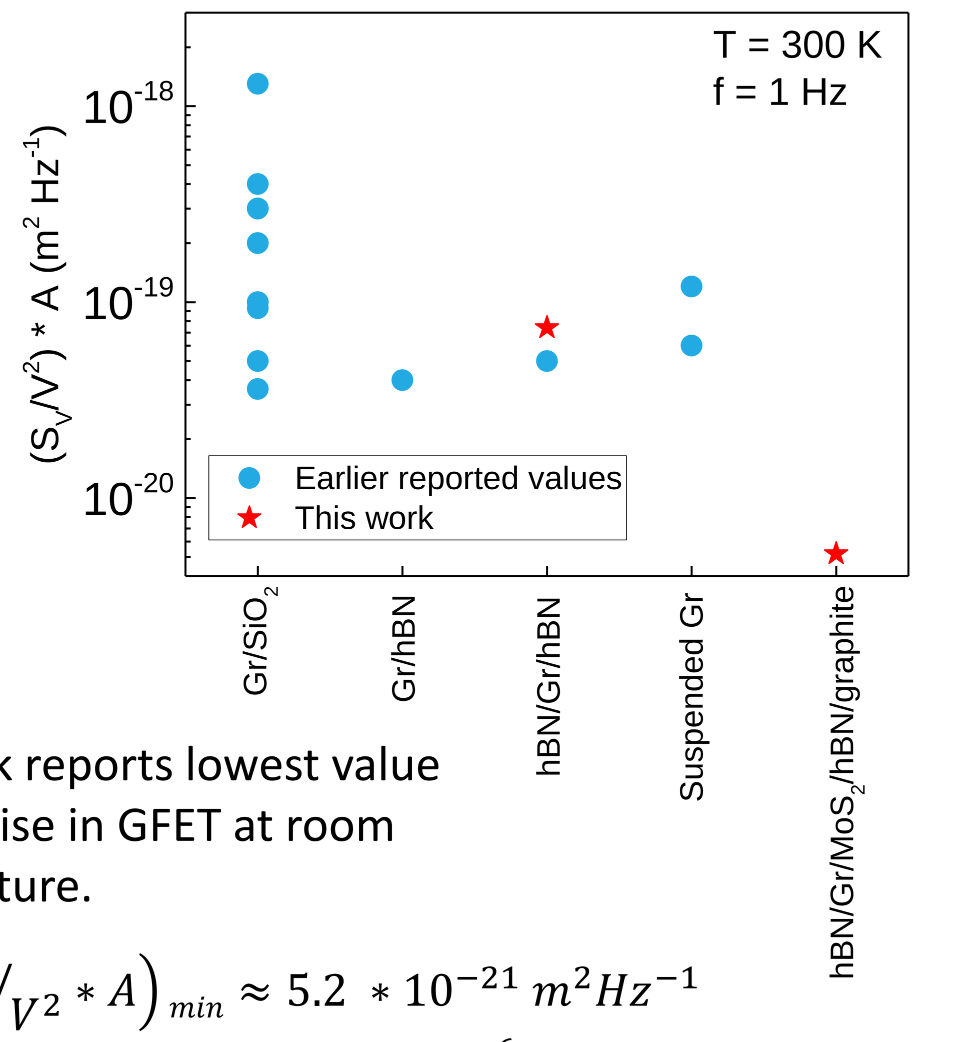
- For $V_G > V_{th}$, screening is increasing (hence noise reduces) with increasing temperature, due to rise in carrier density in MoS_2.



10. Conclusion

- Hall bar geometry, graphite back gate, BN encapsulation and MoS_2 underneath, make graphene transistors with ultra low noise.
- Noise may further be reduced by introducing MoS_2 on top.
- Low noise Gr/MoS_2 hybrid will be crucial in its applications as high-sensitivity optoelectronic element.

9. Comparison with earlier reports



Our work reports lowest value of 1/f noise in GFET at room temperature.

$$\left({S_V}/{V^2} * A\right)_{min} \approx 5.2 * 10^{-21}\, m^2Hz^{-1}$$

$$\gamma_{H,min} \approx 5.2 * 10^{-6}$$

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