Graphene-on-Silicon Hybrid Field-Effect Transistors

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Silicon is an iconic material that has been the cornerstone of micro- and nanoelectronics for the last 50 years. Silicon-based transistors have evolved from being rudimentary and bulky to now having sub-20nm dimensions. *Si* field-effect transistors (FETs) have been extensively used in biosensing applications [1]. However, silicon is known to be a bioresorbable material that gradually degrades when immersed in electrolyte solution. Therefore, Si FETs suffer from a limited operating time. Graphene, on the other hand, has not only opened up new prospects in modern nanoelectronics applications, it also has great potential for bio- and neuro-applications as well as being biocompatible and exceptionally stable in electrolytes [2]. The only drawbacks of graphene are its “leaky” nature (i.e. absence of a bandgap resulting in a large “off” current), and the presence of quantum capacitance that limits the effect of out-of-plane electrical coupling to the biomolecules or electrostatic potentials created by the cells. In this study, we present a new kind of graphene-on-silicon (GoS) structure and use it as a basis for building functional devices, such as FETs. In contrast to Song et al. [3], where GoS-FETs with metal gate were demonstrated, we fabricated liquid-gated structures in which both materials, silicon and graphene, contribute to the transfer of charge. Our study was motivated by the aim of building a hybrid, more robust device that might have an “off” state due to the presence of a silicon mesa structure, yet which exhibits excellent electrical conductivity due to the presence of graphene and is more stable in an electrolytic environment. A large variety of devices were fabricated, with a general schematic shown in Figure 1a, while we varied the widths and lengths of the graphene and silicon channels as well as their ratio and level of silicon doping. We investigate the I–V characteristics of such GoS-FETs. Typical I–V characteristics of a hybrid GoS-FET, bare *Si* FET and bare G FET are shown in Figure 1b. A new working principle of the hybrid device functionality based on the parallel involvement of materials in charge transfer is described.

References

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Figures

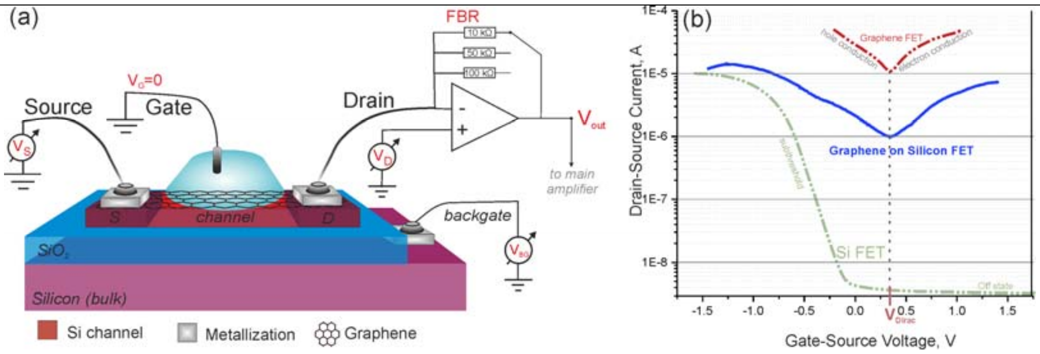

Figure 1: (a) Schematic illustration of a liquid-gated GoS-FET structure; (b) I-V characteristics measured for bare Si FET, bare G FET and hybrid GoS-FET structure