

Low-voltage 2D materials-based printed field-effect transistors on paper

Silvia Conti¹

Lorenzo Pimpolari¹, Gabriele Calabrese¹, Robyn Worsley², Subimal Majee², Dmitry K. Polyushkin³, Matthias Paur³, Simona Pace⁴, Dong Hoon Keum⁴, Filippo Fabbri⁴, Giuseppe Iannaccone¹, Massimo Macucci¹, Camilla Coletti⁴, Thomas Mueller³, Cinzia Casiraghi², Gianluca Fiori¹

¹Dipartimento di Ingegneria dell'Informazione, University of Pisa, Pisa, Italy

²Department of Chemistry, University of Manchester, Manchester, UK

³Institute for Microelectronics (TU Wien), Vienna, Austria

⁴Center for Nanotechnology Innovation (NEST), Pisa, Italy

silvia.conti@dii.unipi.it

Two-dimensional materials are considered excellent building blocks for future every-day electronic applications thanks to their tuneable transport properties and compatibility with flexible substrates, which enable the design of a large variety of devices, ranging from wearable electronics to smart packaging [1]. Here we report high-performance field effect transistors fabricated with a "channel array" VLSI approach. Initially, a pattern of CVD-grown MoS₂ to be used as channels is deposited on paper substrates (Figure 1a). Inkjet printing is then used to complete transistors and circuits fabrication, through the deposition of hBN dielectric layers and silver contacts and connections (Figure 1b). The fabricated devices possess high current modulations (I_{ON}/I_{OFF} up to $> 10^5$) and good mobilities (up to 15 cm²/Vs) [2], comparable with those typical of MoS₂ transistors on rigid substrates (Figure 1c) [3]. Bending tests have shown that the device electrical properties are robust under applied strain. An inverter with high gain, a NAND gate, and a current mirror based on MoS₂ transistors are reported (Figure 2 a, b, c, respectively), showing a path for the development of both analogic and digital circuits for cost-efficient applications.

References

[1] Z. Lin, Y. Huang, X. Duan, *Nature Electronics*, 2 (2019) 378-388.

[2] S. Conti *et al.*, [arXiv:1911.06233v1](https://arxiv.org/abs/1911.06233v1)

[3] S. Park, D. Akinwande, 2017 IEEE International Electron Devices Meeting (IEDM), (2017)

Figures

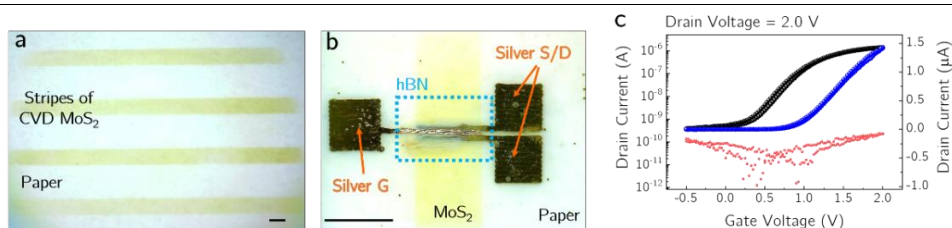


Figure 1: Optical micrograph showing the transferred MoS₂ stripes on paper (a). Inkjet-printed transistors on paper (b). The scale bars in a-b correspond to 500 μ m. Typical transfer characteristic curve (c). Logarithmic scale: black dots, drain current; golden dots, gate current. Linear scale: blue dots, drain current.

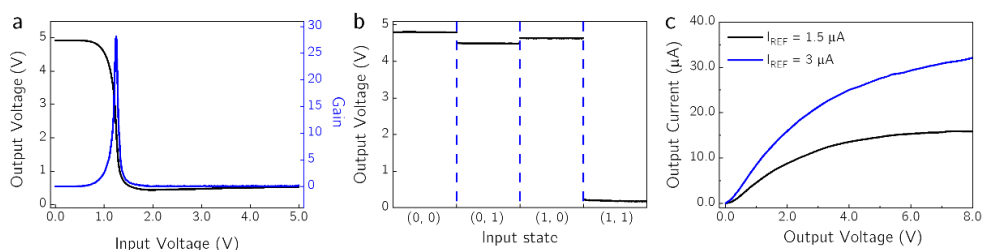


Figure 2: Input-Output characteristic (left axis) and voltage gain (right axis) of an inverter gate as a function of the input voltage (a). Output voltage of the NAND gate as a function of the input states (b). Output current of the current mirror as a function of the output voltage for two different values of the reference current (c).