Graphene field effect transistors using TiO_2 as the dielectric layer

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Graphene based electronic devices face the challenge to find a suitable dielectric material which has little or negligible effect in diminishing graphene's interesting properties, such as electron and hole mobility and ambipolar effect. In this sense, titanium dioxide (TiO_2) is a promising insulator material which adapted with graphene could lead to better performance of graphene based devices. In this work [1], we manufactured three Graphene Field Effect Transistors (GFETs) using a thin deposit of TiO_2 as the dielectric layer. Characterization of the devices was done by measuring resistance between electrodes vs gate voltage, data was then fitted to the model proposed in the literature [2] taking electron/hole mobility, contact resistance and charge carrier density as adjusting parameters. We observed that, due to the high dielectric constant (14.0 [3]) of the TiO_2, the Dirac voltage or charge neutrality point of our three GFETs has been decreased to nearly 0V in the gate, compared to other similar devices which use SiO_2 (dielectric constant of 3.8 [4]), with the Dirac voltage appearing at nearly -15V. Thus, the device being able to show the ambipolar effect at very low voltages applied in the gate, as shown in Figure 1. We also show that it is possible to manufacture GFETs with good electron and hole mobility values (up to 1870 cm^2/Vs) using a large graphene area channel (300x300 μm^2), knowing that it conveys a greater number of defects and wrinkles, generally. Photographs of the manufactured devices are shown in Figure 2. Finally, it is presented a qualitative description of the electron and hole mobilities behavior in dependence of the roughness of the dielectric layer, finding these mobilities to be decreased as the roughness increases, as expected; and thus determining that the dielectric layer roughness is an important parameter which could introduce large undesirable effects in the device performance.

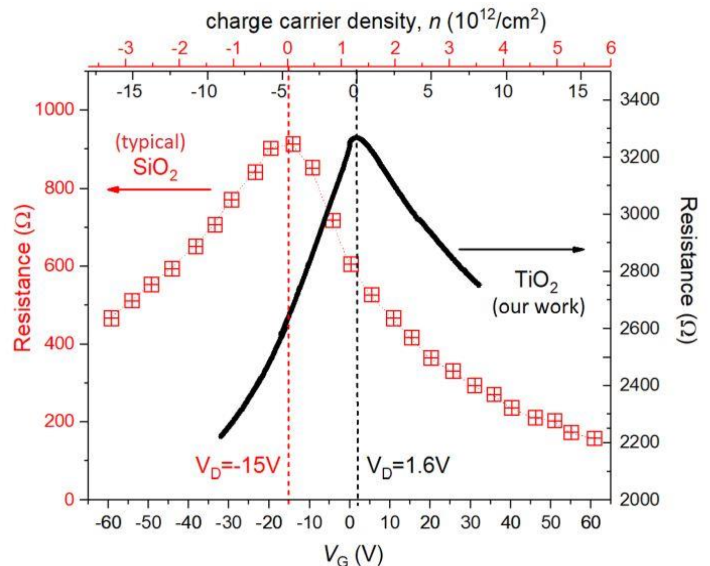

Figure 1: Resistance vs gate voltage plot for our GFET (black line) compared to one using SiO_2 as dielectric layer (red boxes).

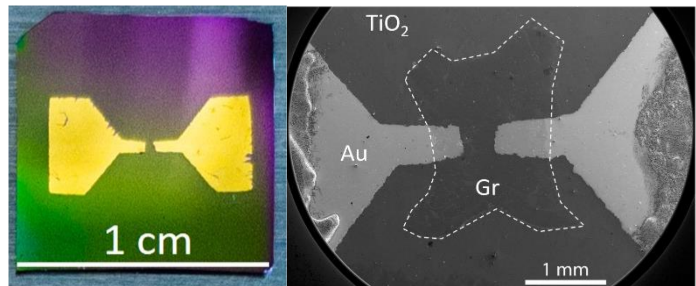

Figure 2: (a) Photograph of one GFET fabricated with Au(150nm)/Cr(15nm) electrodes. (b) SEM image of the graphene channel area.

[1] Flores-Silva et al. Physica E 124 (2020) 114282.
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[3] M. Takeuchi, et al. Thin Solid Films 51 (1978) 83–88.
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