Optimal architecture for ultralow noise graphene transistors at room temperature

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The fundamental origin of low-frequency noise in graphene field effect transistors (GFETs) has been widely explored but a generic engineering strategy towards low noise GFETs is lacking. Here we systematically study and eliminate dominant sources of electrical noise to achieve ultralow noise GFETs. We find that in edge contacted, high-quality hexagonal boron nitride (hBN) encapsulated GFETs, the inclusion of a graphite bottom gate and long (> 1.2 μm) channel-contact distance significantly reduces noise as compared to global Si/SiO_2 gated devices. From the scaling of the remaining noise with channel area and its temperature dependence, we attribute this to the traps in hBN. To further screen the charge traps in hBN, we place few layers of MoS_2 between graphene and hBN, and demonstrate that the noise is as low as $\sim 5.2*10^{-9}$ μm^2 Hz^{-1}(corresponding to minimum Hooge parameter $\sim 5.2*10^{-6}$) in GFETs at room temperature, which is an order of magnitude lower than the earlier reported values.