Ultra-scaled MoS_2 FETs

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Silicon based electronic devices are rapidly approaching scaling limits. Further scaling of field-effect transistors (FETs) requires atomically thin semiconducting channels. The atomic thickness of two-dimensional materials (such as MoS_2) make them ideal candidates for replacing Si in ultra-short (gate length ~ 10 nm) FETs [1]. However, large scale fabrication of ultra-short FETs have been challenging. There have been several attempts to realize ultra-short MoS_2 FETs but they comprised several short-channel FETs connected in series [2] or had very long access areas around the gate [3,4], making actual device dimensions much larger. A true ~ 10 nm MoS_2 FETs have been recently reported [5-6], but using random cracks or grain boundaries which are unsuitable for large-scale device fabrication.

Here we demonstrate ultra-short channel MoS_2 FETs fabricated on a large scale without nanolithography. We used shadow evaporation method to fabricate FETs with a channel length as short as 10 nm. The FETs were realized both with exfoliated few-layer MoS_2 (thickness ~ 7 nm) and monolayer MoS_2 grown by chemical vapour deposition as channel material. The 10 nm MoS_2 FETs exhibited drain current on/off ratio > 10^5 and maximum drain current ~ 560 A/m, which is the highest drain current reported in MoS_2 FETs until now. The smallest subthreshold swing was 120 mV/dec. The FETs exhibited a very good drain current saturation (output conductance ~ 2 S/m) for such short-channel devices.

We also demonstrated logic inverters in depletion mode technology using the 10 nm MoS_2 FETs. The inverters exhibited a voltage gain as high as 20 and were capable of in/out signal matching.

References

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Figures

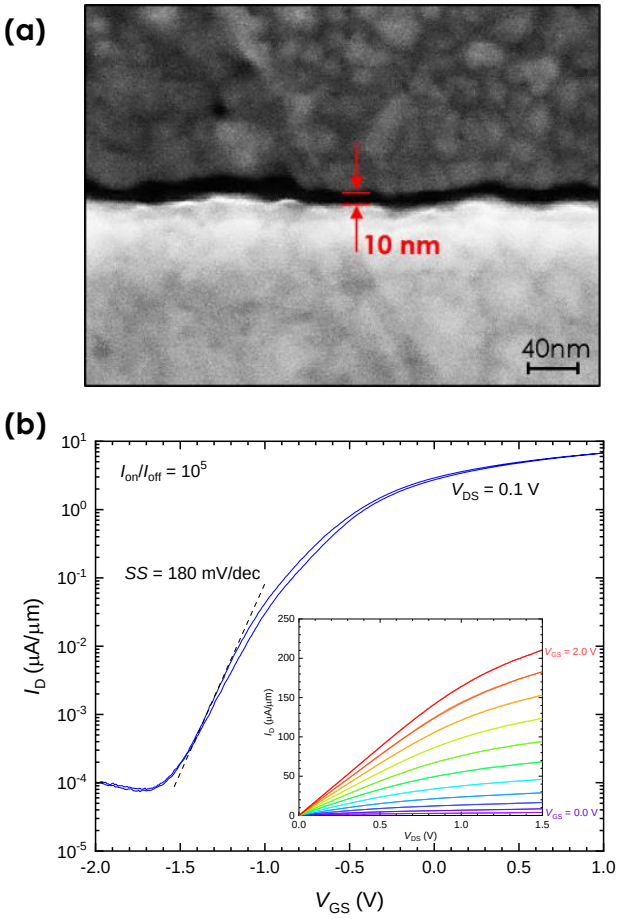

Figure 1: (a) SEM micrograph of an MoS_2 FET with a channel length of 10 nm. **(b)** Transfer curve of a 10 nm FET at 0.1 V of drain-source voltage (V_{DS}). Subthreshold swing of this FET is 180 mV/dec. Inset shows output curves of a 10 nm FET at different gate-source voltages (V_{GS}).