

Graphene monolayer treated with UV irradiation for large area FETs by optimized electron beam lithography

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Abstract

We present our preliminary results on the fabrication of large area bottom gate MOSFETs, suitable for sensors. In order to achieve high performance MOSFET devices we optimized the graphene transfer procedure onto 10nm SiO₂ layers, thermally grown on n⁺-Si (~0.003 Ω.cm) wafers. Monolayer graphene grown on copper substrates by chemical vapour deposition (CVD) was transferred using a supporting PMMA layer. Optimization of Cu etching process and PMMA cleaning was thoroughly investigated by Raman measurements. Graphene channel was defined by dry etching, while source/drain Pt contacts were sputtered and formed by metal lift-off. Raman studies in large areas of graphene films revealed that the used UV assisted cleaning method after transfer improves material's performance. More specifically, transfer characteristics revealed that graphene is p-doped and thus the current under negative gate bias is significantly higher than the current under positive bias. The Dirac point was shifted about +3V and no-hysteresis was observed either in I_{ds}-V_{gs} or I_{ds}-V_{ds} characteristics. Both findings suggest relatively low density of trapped charges at the graphene/oxide interface. The extracted field effect mobility for electrons was found about 1300 cm²/Vs while for holes it was about 2000 cm²/Vs. Finally, we didn't

observe significantly degradation of the device performance after several months.

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References

- [1] A. Das *et al.* Nat. Nanotechnol., 3, 210–215 (2008)
- [2] G. Anagnostopoulos *et al.*, ACS Applied Materials & Interfaces, 2016.

Figures

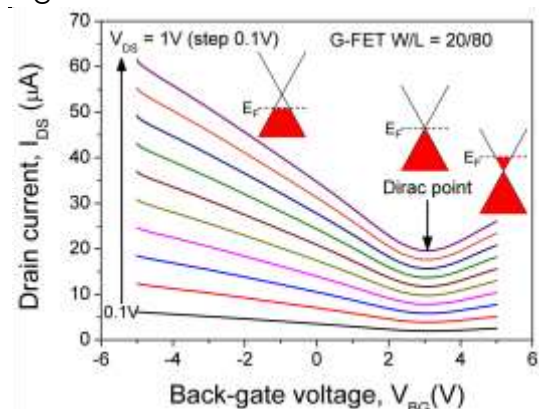


Figure 1: Transfer characteristics measured at different source-drain voltages.

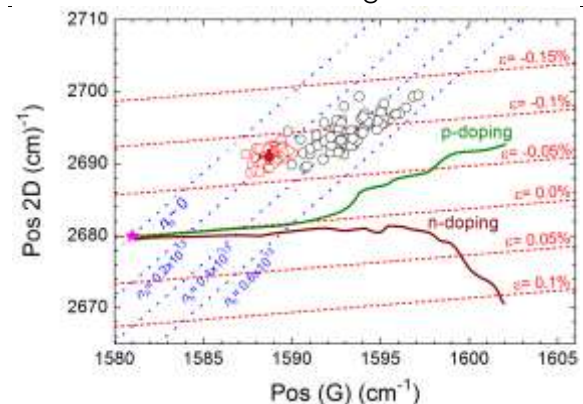


Figure 2: Pos(G) vs Pos(2D) of CVD graphene samples on top of Si/SiO₂ substrate. The doping data are taken from [1], while the mechanical strain is considered pure biaxial.