Graphene in 200 mm CMOS Fab: challenges and perspectives

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Due to the unique properties of graphene, a large number of various graphene-based microelectronic devices have been proposed [1-2]. Recent demonstrations of graphene devices on a wafer scale [3-5] clearly indicate the potential of the graphene technology but at the same time raises questions concerning the manufacturability, as well as the integration and compatibility with Si technology. From this point of view, the investigation and preparation of graphene devices in conditions resembling as close as possible the Si technology environment is of highest importance.

In this paper, we present the attempts to integrate graphene into the 200mm silicon technology platform. We investigated the processes of graphene synthesis on silicon compatible materials like germanium (Fig.1), its large area transfer, cleaning, patterning, a non-destructive deposition of dielectric materials on the graphene sheet as well as the combinations of these processes for various concepts of contacting graphene on full 200 mm wafers (Fig. 2). Finally, we point out the challenges and roadblocks which need to be overcome to enable the integration of graphene with Si devices.

References

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Figures

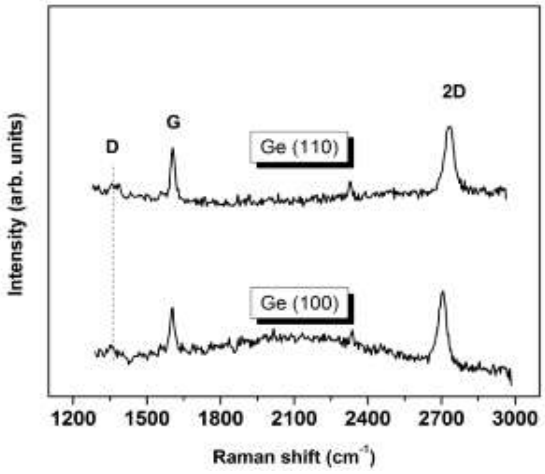

Figure 1: Raman spectra acquired on 200 mm Ge(001)/Si(001) and Ge(110)/Si(110) substrates.

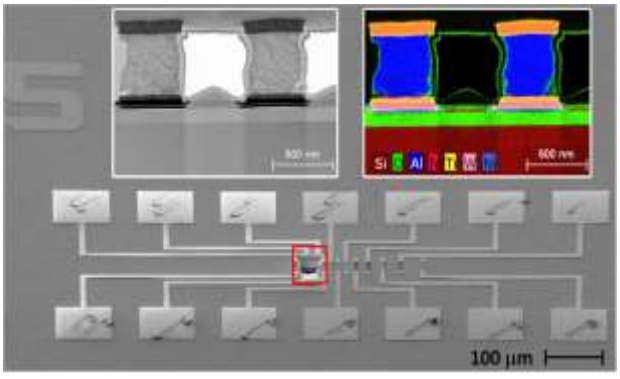

Figure 2: Tilted SEM view of a TLM device with graphene. STEM (inset left) and EDX (inset right) analysis.