2D material roadmap to integrated technology : from lab to CMOS fab.

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2D materials are considered as an additional active material in the semiconductor integration portfolio[1]. Indeed their 2D nature makes them natural candidates for monolithic integration which opens the door for density scaling and system technology co-optimisation along the 3rd dimension at reasonable costs. The application space ranges from replacement for Si in advanced nodes, over smart- and optical interconnects and sensor and imager applications.
In the talk we will highlight the challenges and options to consider towards a scaled 2D integrated solution. For different key challenges, we will benchmark possible integrated solutions. Finally we report the learning from our first lab to fab vehicle designed to bridge the lab and imec's 300mm pilot line[2].

References

[1] Cedric Huyghebaert *et al.*, "2D materials: roadmap to CMOS integration," presented at the IEDM 2018, San Fransico.
[2] T. Schram *et al.*, "WS2 transistors on 300 mm wafers with BEOL compatibility," in *2017 47th European Solid-State Device Research Conference (ESSDERC)*, 2017, pp. 212–215.

Figures

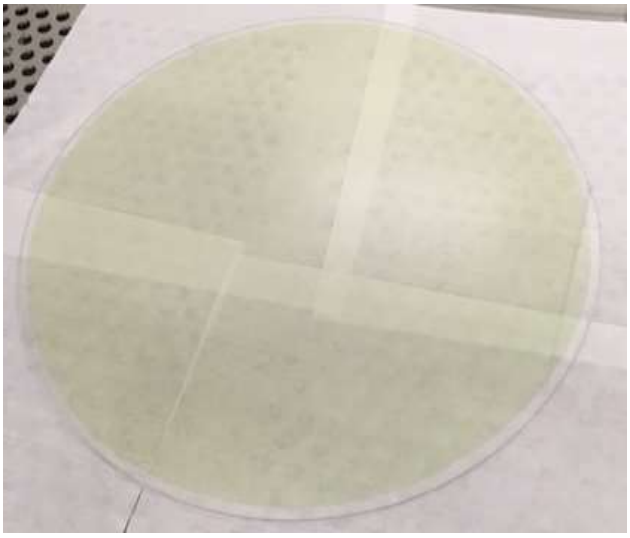

Figure 1: 300mm WS_2 layer transferred on a glass carrier.

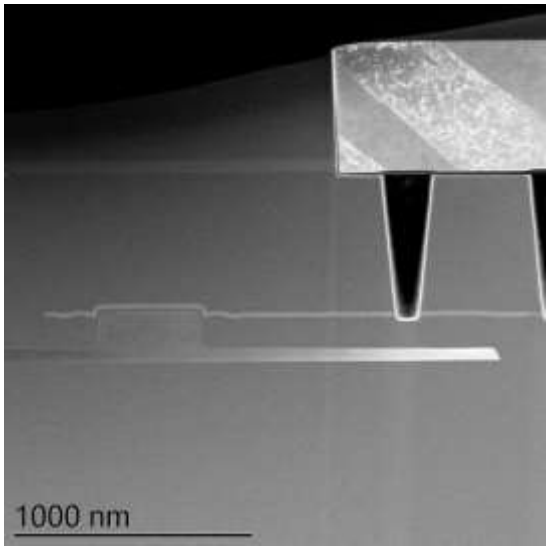

Figure 2 : TEM image of a graphene on Si modulator contacted through a damascene module