Two-Dimensional Materials Inserted at the Metal/Semiconductor Interface: Attractive Candidates for Semiconductor Device Contact

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Scaling of complementary metal–oxide–semiconductor (CMOS) is of great importance for achieving optimal packing density and device performance. With much research efforts and the development of various strategies such as high-k/metal gate and fin-type field-effect transistor (FinFET) structure, the current CMOS technology has reached up to 10 nm in the channel length regime. However, recently, the progress in CMOS technology has slowed down, and the technology is facing critical challenges. One of the major challenges in further scaling of CMOS is reducing the contact resistance at the metal–semiconductor interface, which causes the deterioration of the device performance such as high operating voltage, high power dissipation, and low device operating speed. Ultimately, according to the international technology roadmap for semiconductors (ITRS) roadmap, sub-nΩ•cm^2 specific contact resistivity (ρc) is required under 10 nm node.

Meanwhile, 2-dimensional (2D) materials such as graphene, hexagonal boron nitride (h-BN), and transition metal dichalcogenides (TMD) have emerged as good candidates for the interfacial layer because they have a crystalline structure, a one atomic thickness, and high thermal stability (> 800 °C). However, there has been no systematic investigation on the ρc of metal/2D material/Si (M/2D/Si) systems in terms of the integration process and the pinning effect based on various metals.

In this presentation, we propose a new method to reduce the SBH and Rc at the metal/Si interface with the insertion of semiconducting 2D materials, such as graphene, h-BN, and transition metal dichalcogenides. In this approach, an interface dipole formed at the metal-2D interface modulate the work function of metal to align with the conduction band edge of Si, leading to the reduction of SBH and the Rc. We obtain SBH of less than 0.2 eV with a proper choice of interlayer materials. We also simulate the Schottky barrier height of 2D inserted metal/Si interfaces and the results are in good agreements with experimental results.