# Challenges of large area integration of 2D materials in CMOS line

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We established an integration module for 2D materials in the 300mm line. We demonstrate the integration of graphene and MX2-based transistors using standard state of the art production tools[1]. The 2D material was directly deposited atomic layer deposition (ALD) or growth on a template surface and transferred to the pre-processed target wafer. The major integration challenges are the limited adhesion and the fragility of the (few)monolayer 2D material.
The wafer level 2D material transfer, consisting of delamination from substrate and lamination on target wafer, is poorly understood and a key factor to the success of this 2D platformization effort. We will discuss the most recent insights on the role of ions in liquids on adhesion of 2D materials[2-3].

The delamination issues during integration are mitigated by using a sacrificial $Al_2O_3$ capping layer and by sealing the edges of the 2D material before wet processing. The 2D material channel is contacted with Ti/TiN side contacts and an industry-standard back end of line (BEOL) flow. This novel low-temperature flow is the first step for the integration 2D devices in the BEOL CMOS applications according to the industry standards.

## References

[1] Toms Schram et al., Essderc 2017 conference proceedings : http://ieeexplore.ieee.org/document/8066629/.
[2] Ken Verguts et al., ACS Applied Materials & Interfaces vol 9 issue 42 (2017) p37484
[3] Verguts et al., Nanoscale 10(12), (2018)

## Figures

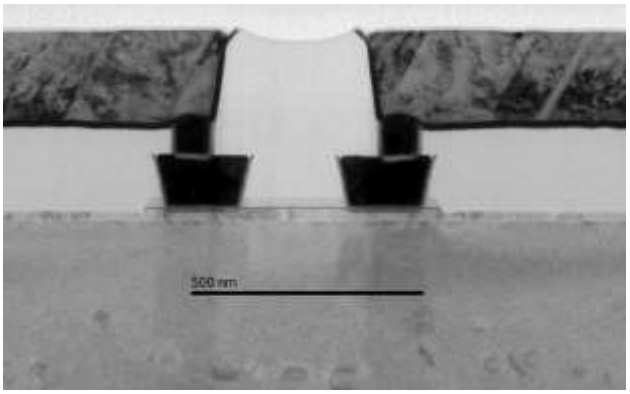


**Figure 1:** TEM image of $WS_2$ backgated transistor contacted through a damascene Ti/TiN/W side contact integration module. The $Al_2O_3$ encapsulation layer can clearly be seen between the contacts[1].

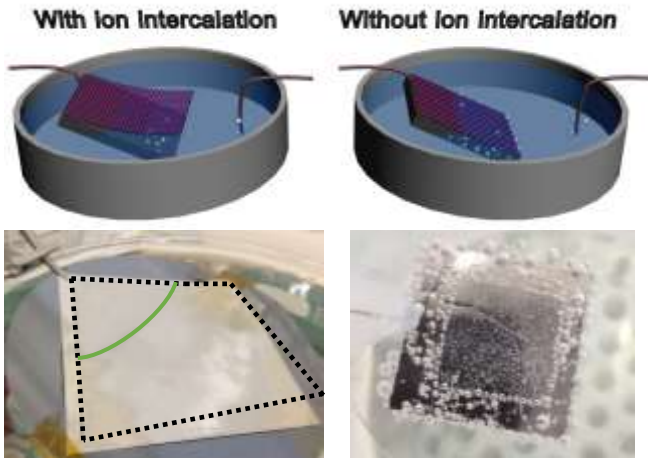


**Figure 2:** Left: Graphene delamination is successful in Na+, K+, TMA+ and TEA+ containing electrolytes. Right: Although hydrogen bubble formation is observed, graphene could not delaminate in H+, NH4+ or Ce4+ containing electrolytes. [3]